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GaN Transistors for Efficient Power Conversion

April 22-25, 2013
McEnery Convention Center
San Jose, CA
www.ubmdesign.com

EPC
EFFICIENT POWER CONVERSION

UBM
Tech

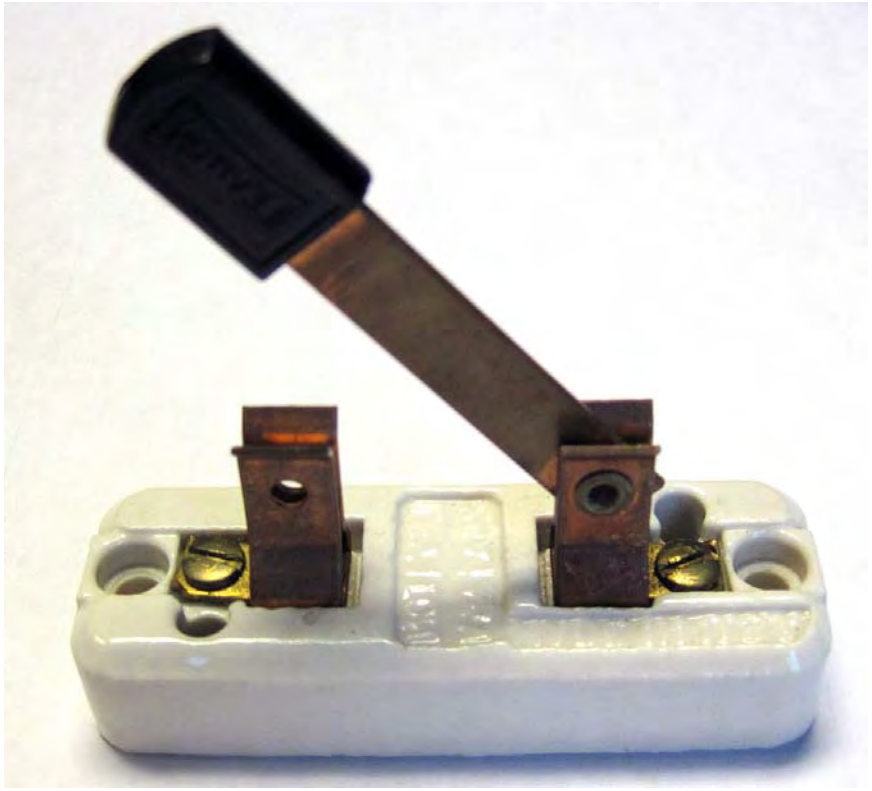
Agenda

- How GaN works
- Electrical Characteristics
- Design Basics
- Design Examples
- Summary

How GaN Works

The Ideal Power Switch

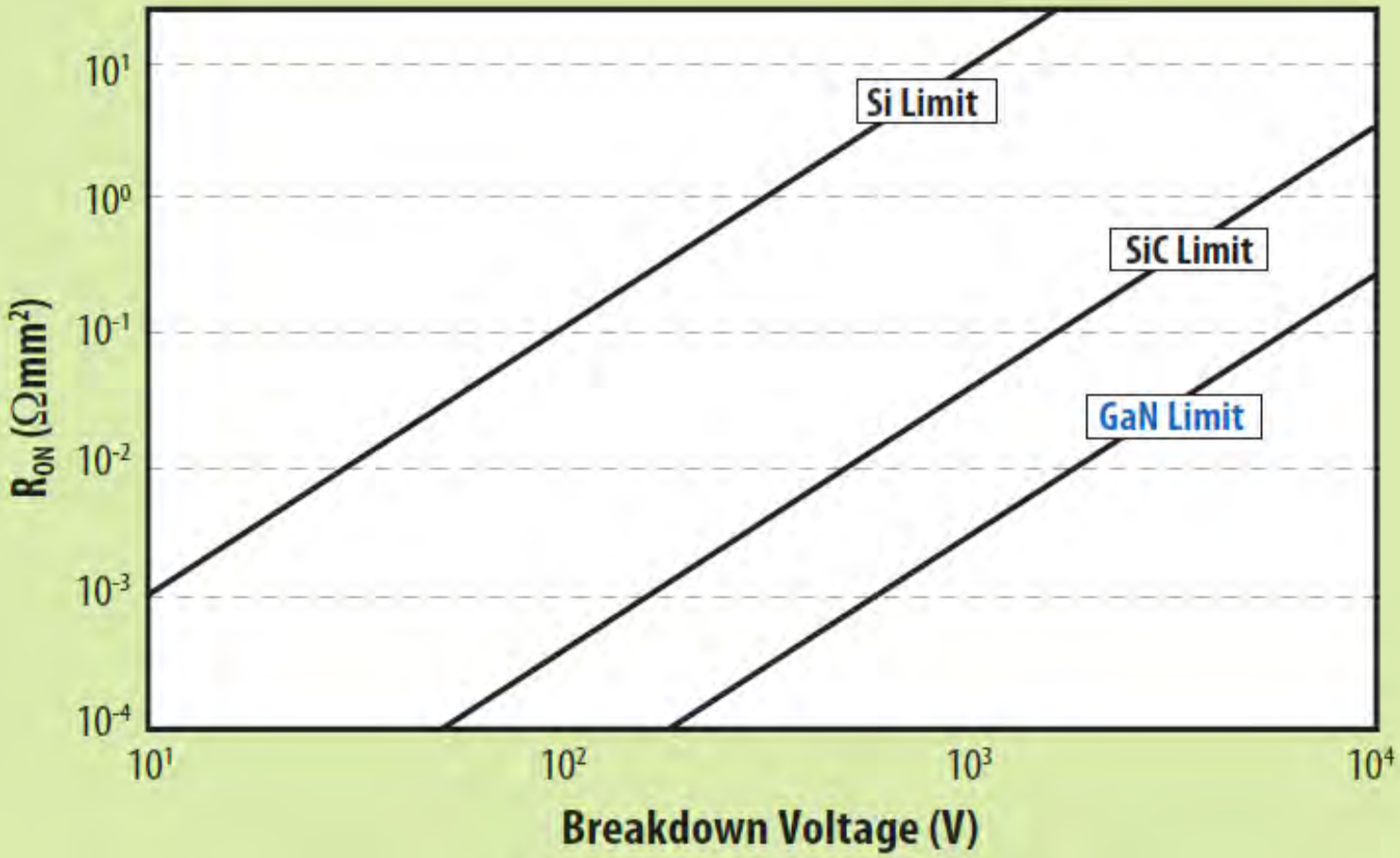
- Block Infinite Voltage
- Carry Infinite Current
- Switch In Zero Time
- Zero Drive Power
- Normally Off



Power Switch Wish List

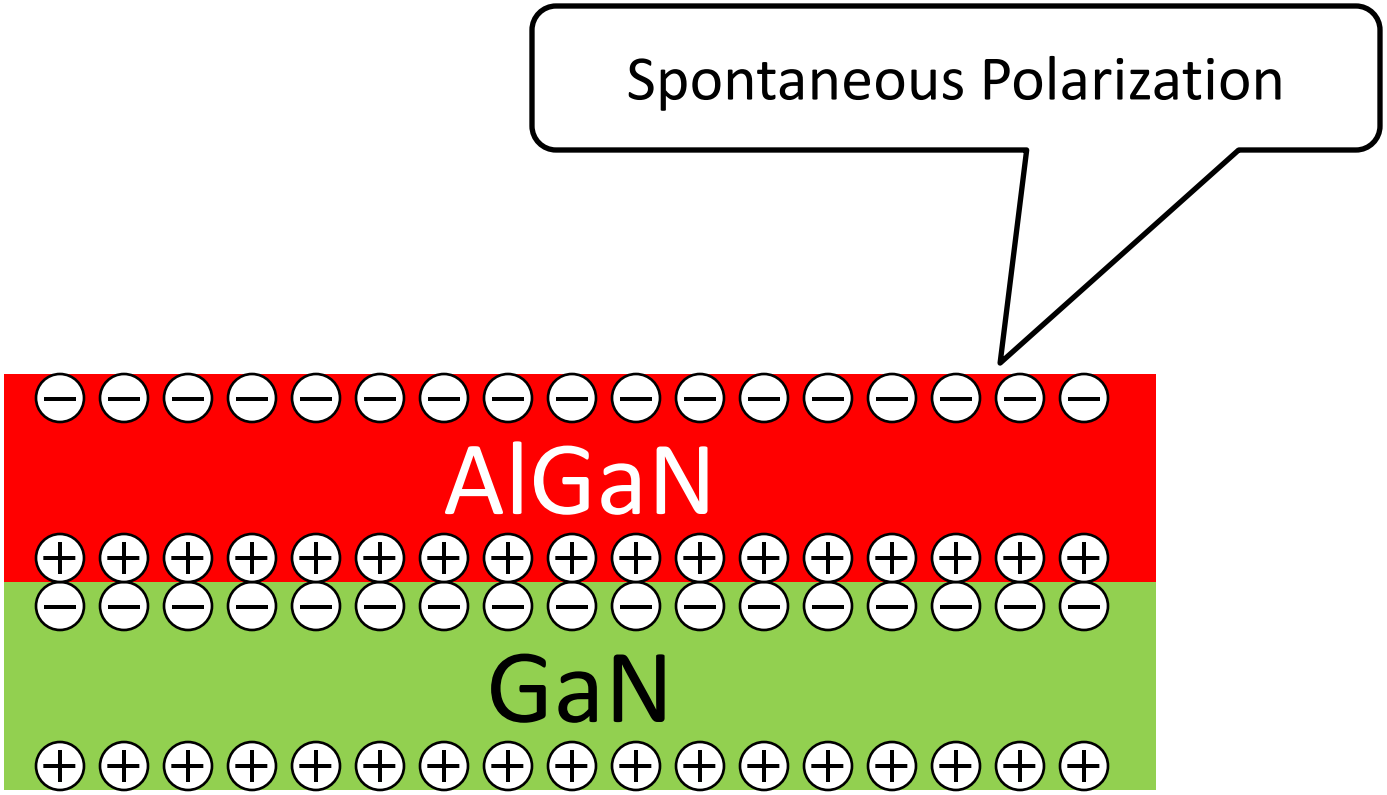
- Faster
- Lower Conduction Loss
- Less Capacitance
- Smaller
- Lower Cost

Material Comparison

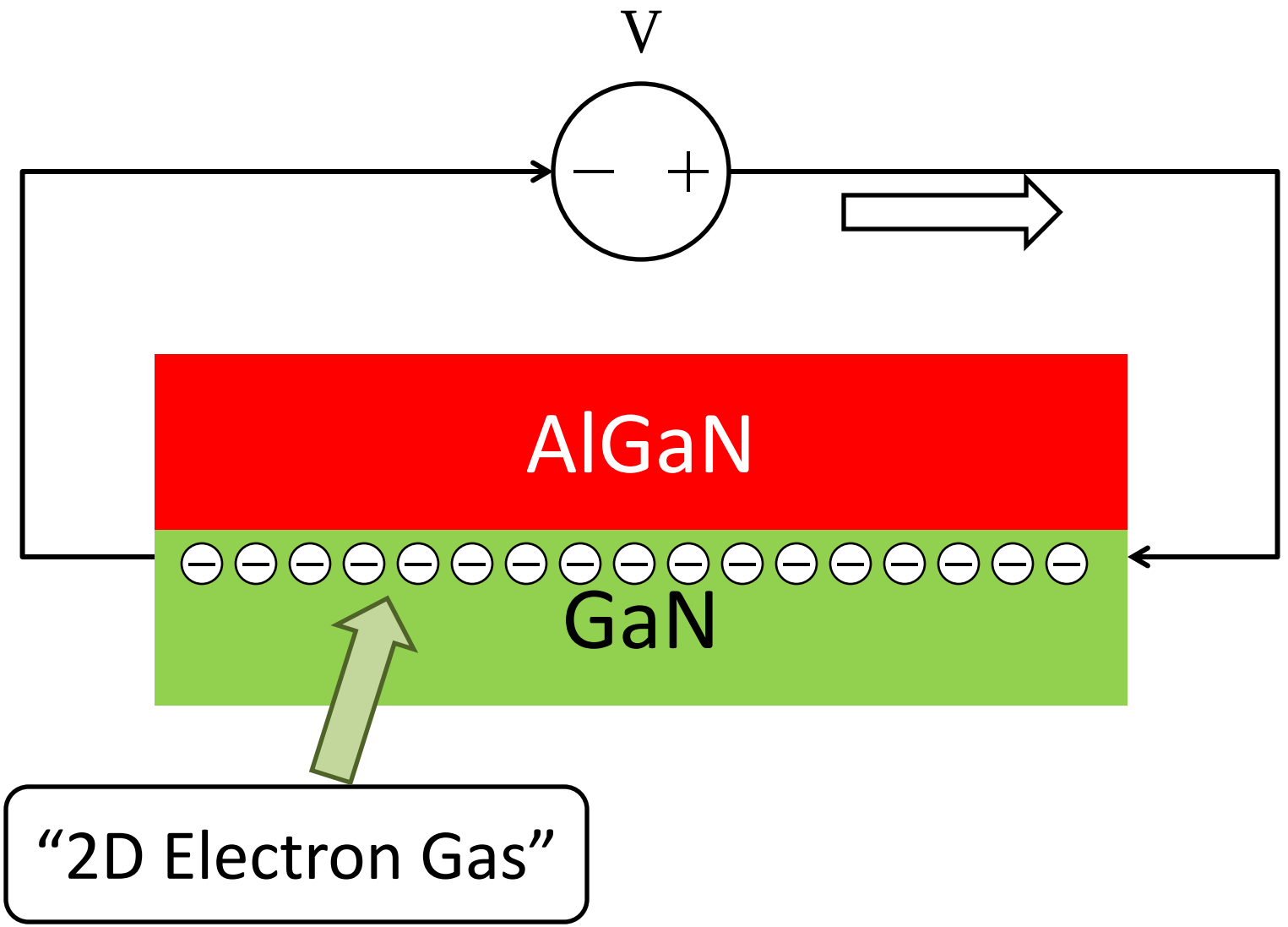


Theoretical on-resistance vs blocking voltage capability for silicon, silicon-carbide, and gallium nitride

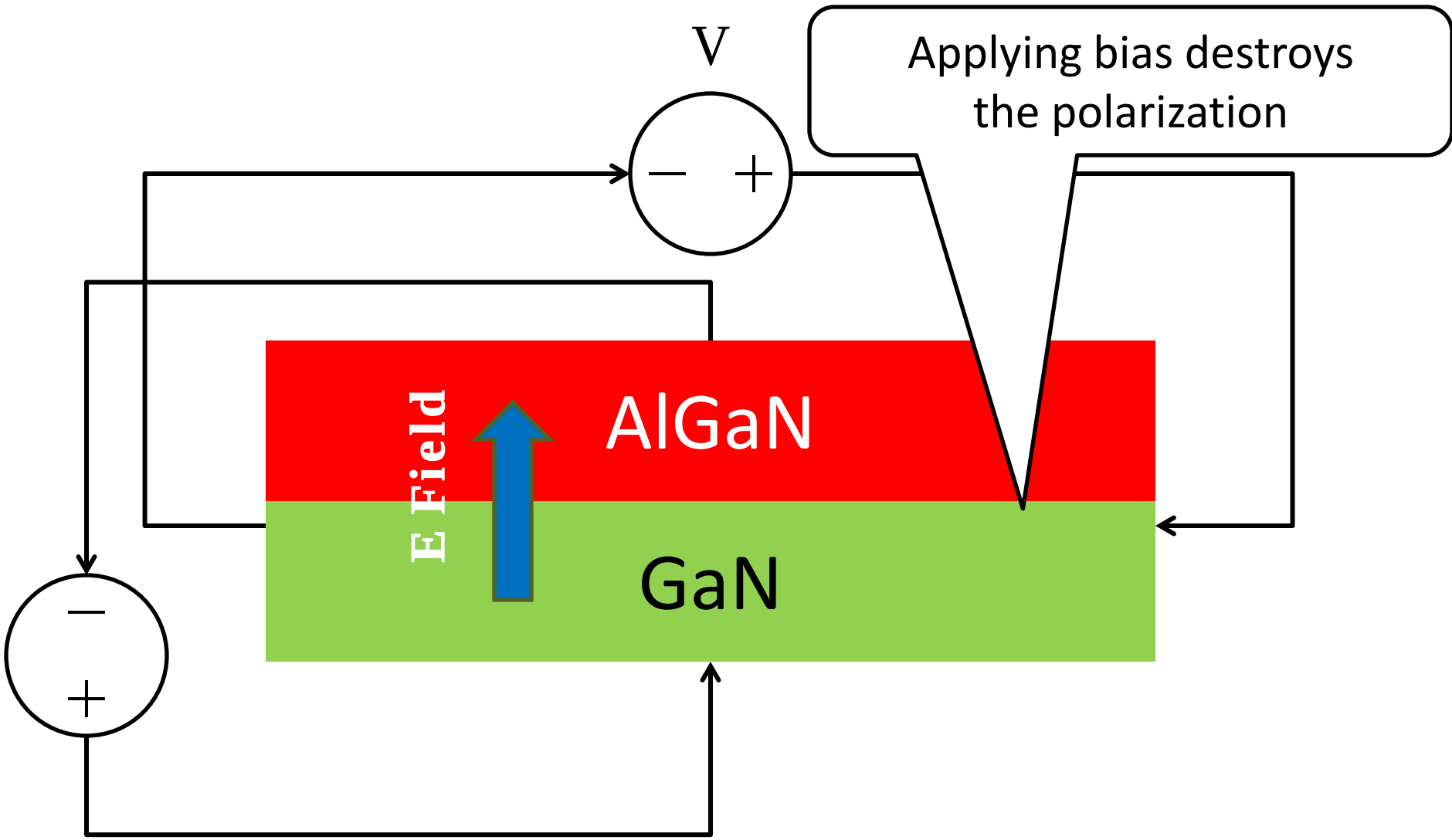
GaN + AlGaN



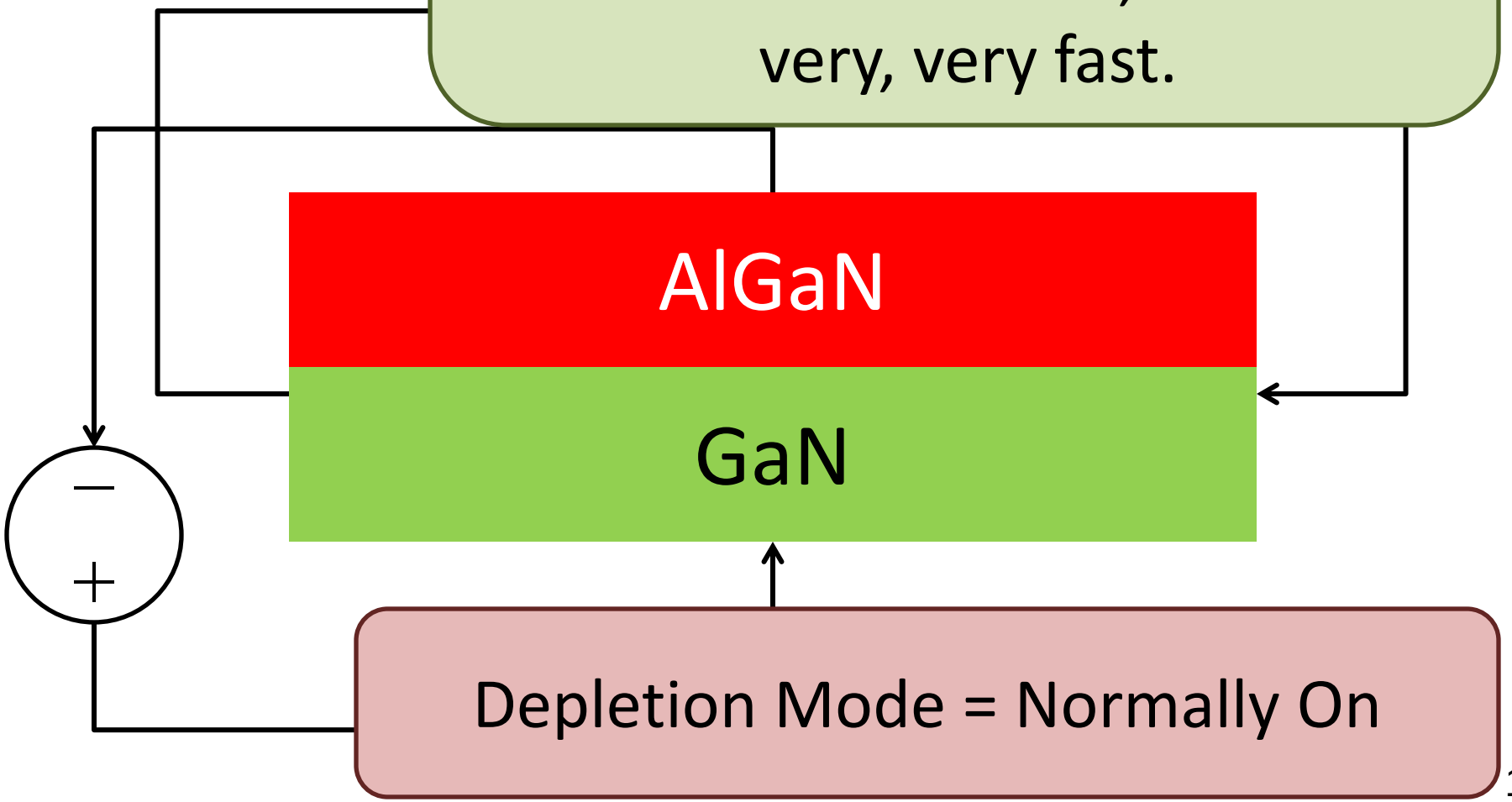
GaN Magic



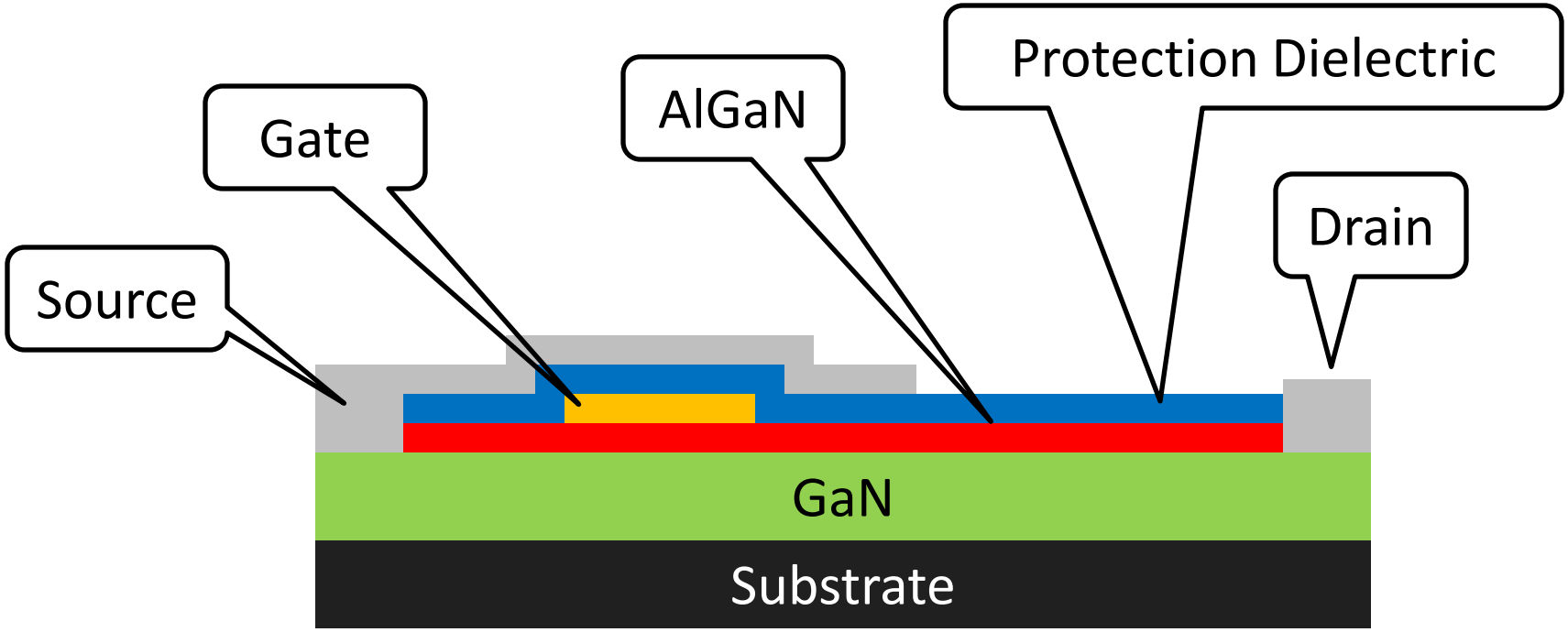
GaN Switch


V
Applying bias destroys the polarization
E Field
AlGaN
GaN

Now we have a switch
That has high voltage blocking capability,
low on resistance, and is
very, very fast.



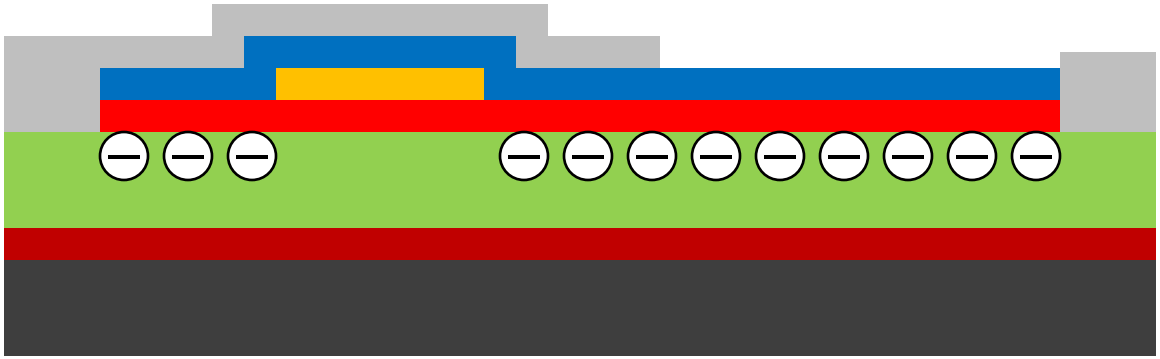
Device Construction Concept



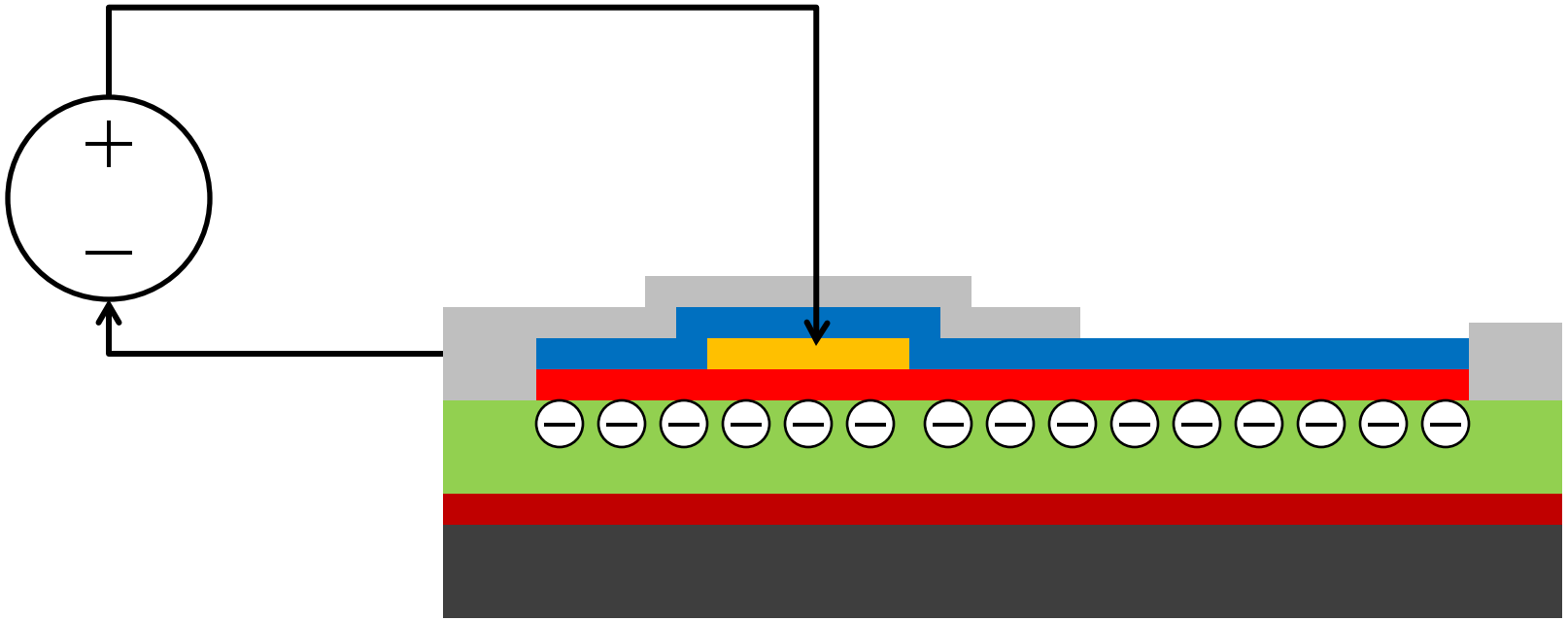
Early substrate materials: SiC and Sapphire Are expensive and hard to manufacture. Silicon substrates are much lower cost and allow fabrication in a standard CMOS Fab.

What About Normally Off Devices?

- True enhancement mode GaN HFETs have been around for years
- There are various methods for dissipating the electron gas under the gate

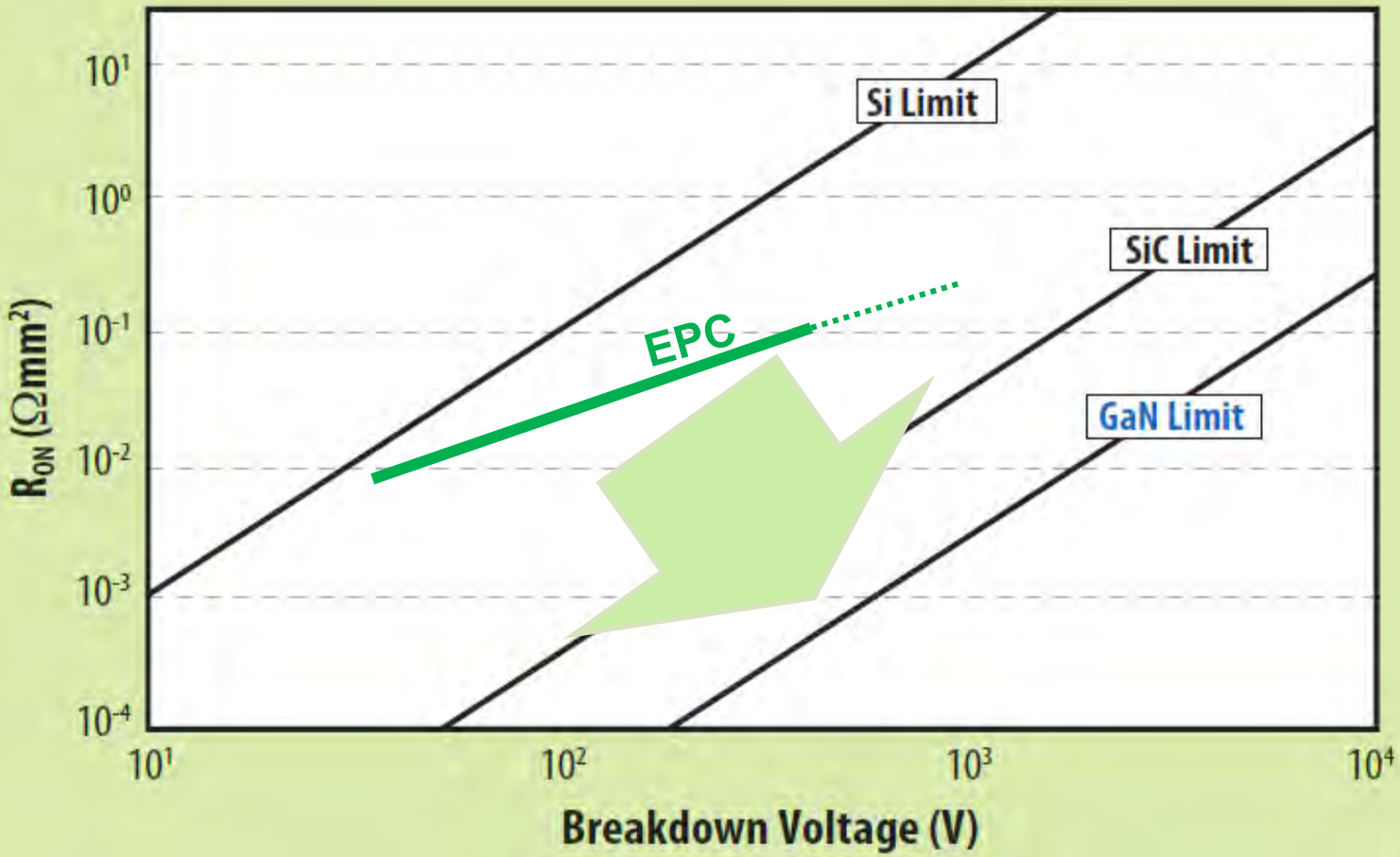


Enhancement Mode



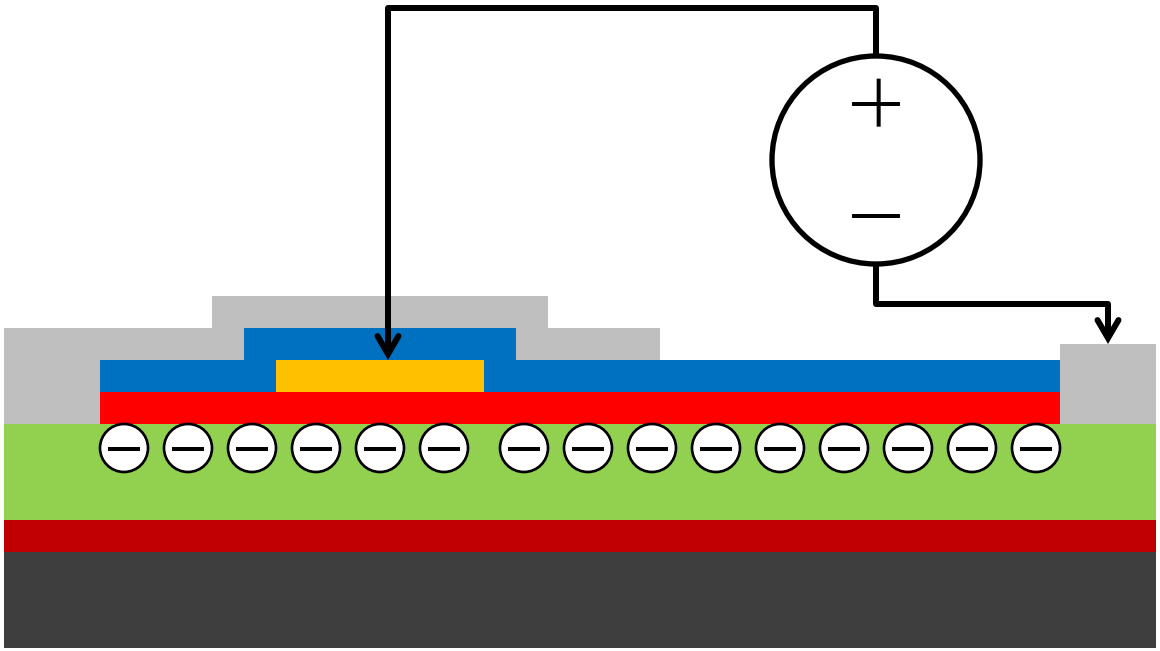
A positive voltage from Gate-To-Source establishes an electron gas under the gate

State of the Art



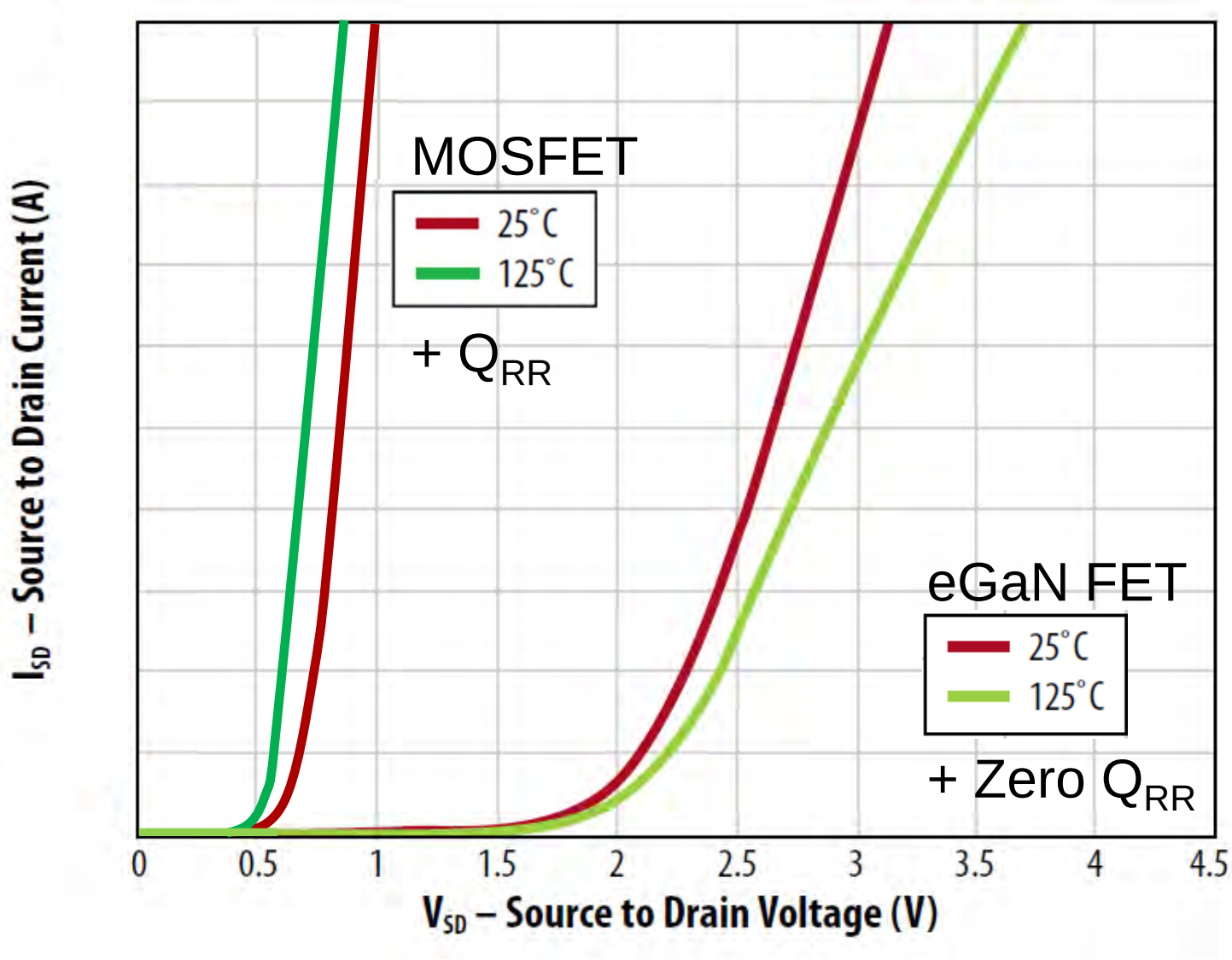
Theoretical on-resistance vs blocking voltage capability for silicon, silicon-carbide, and gallium nitride

Body Diode?

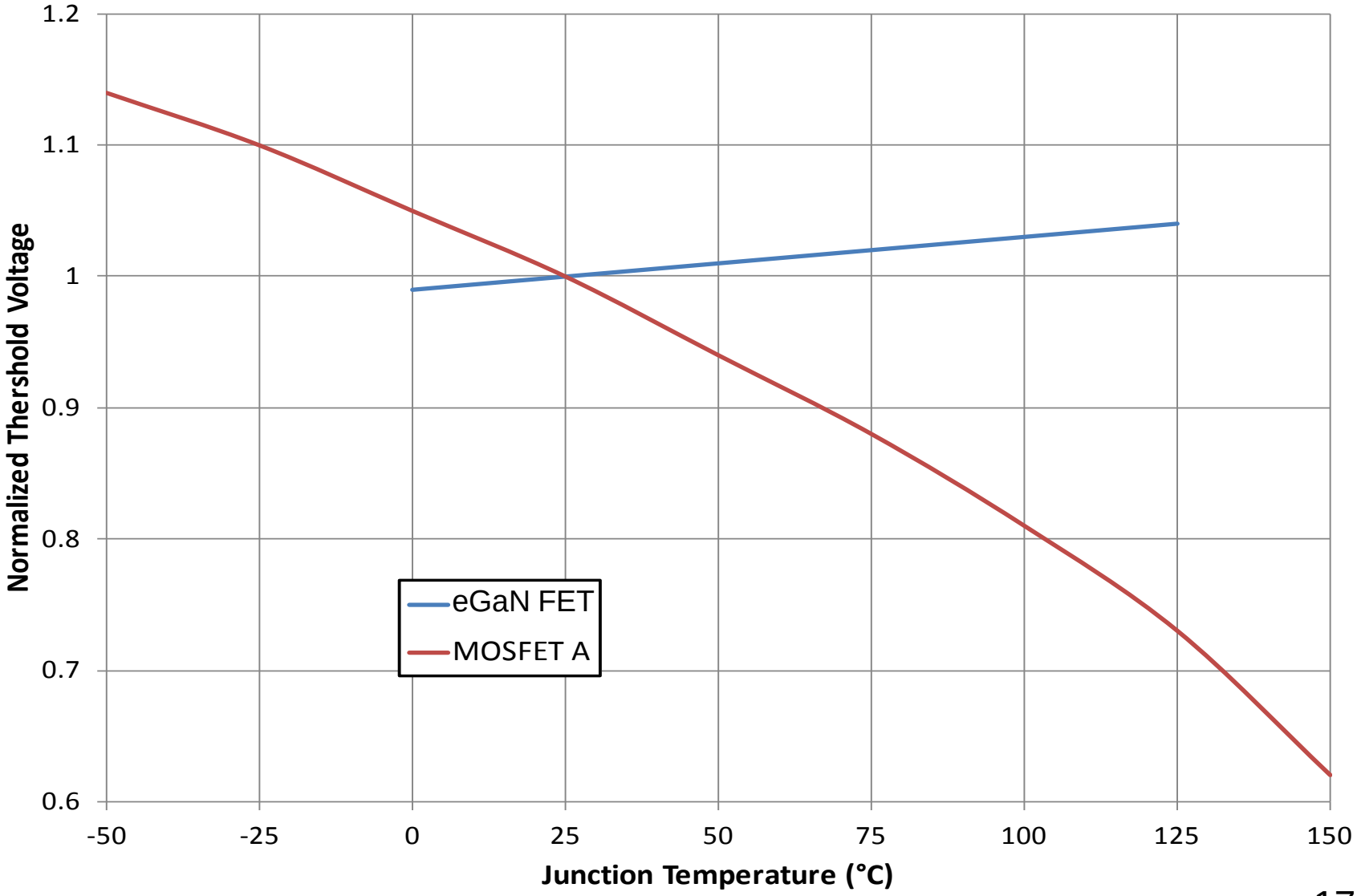


A positive voltage from Gate-To-Drain
also establishes an electron gas under the gate

eGaN® FET Reverse Conduction

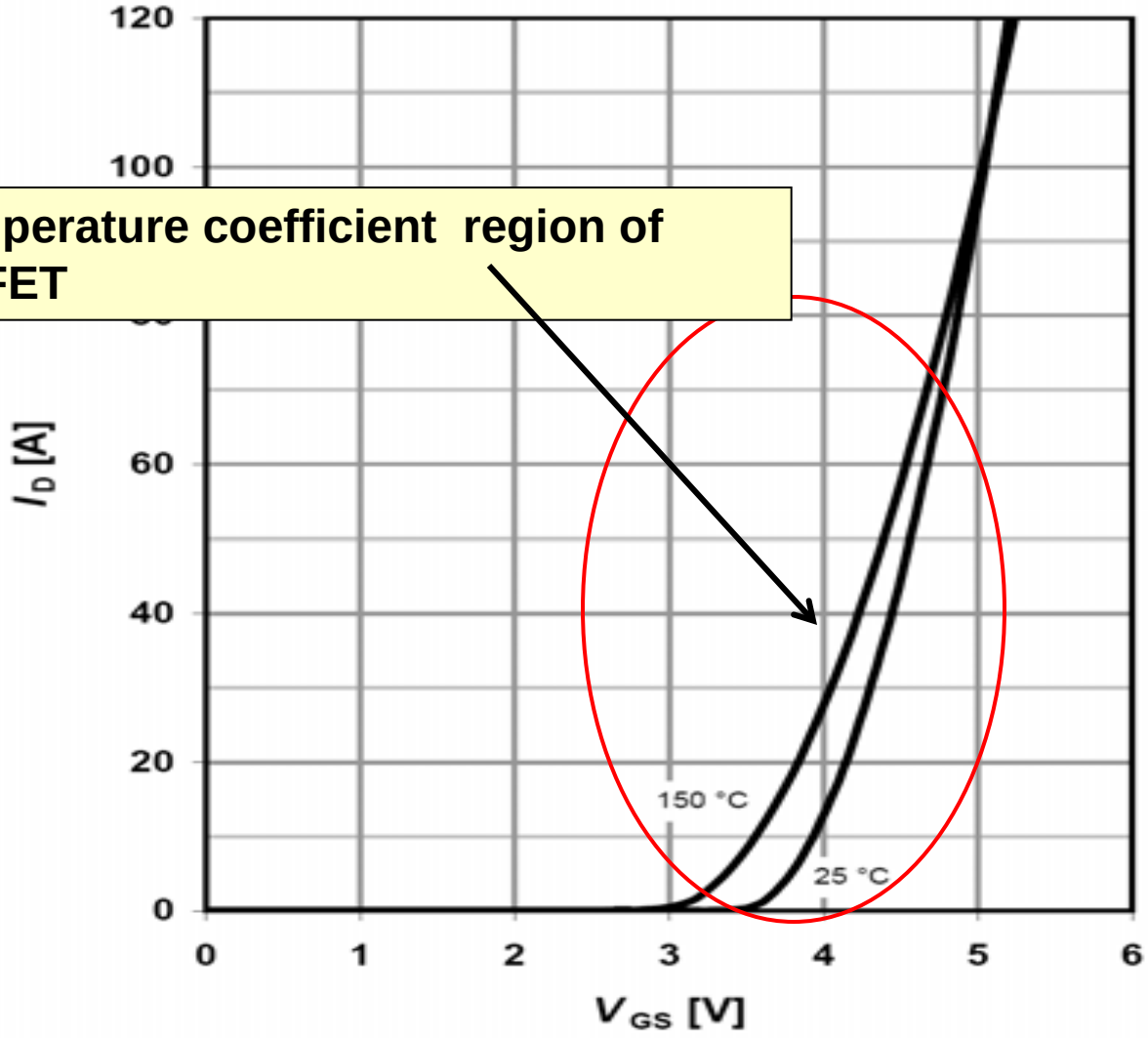


Threshold vs. Temperature



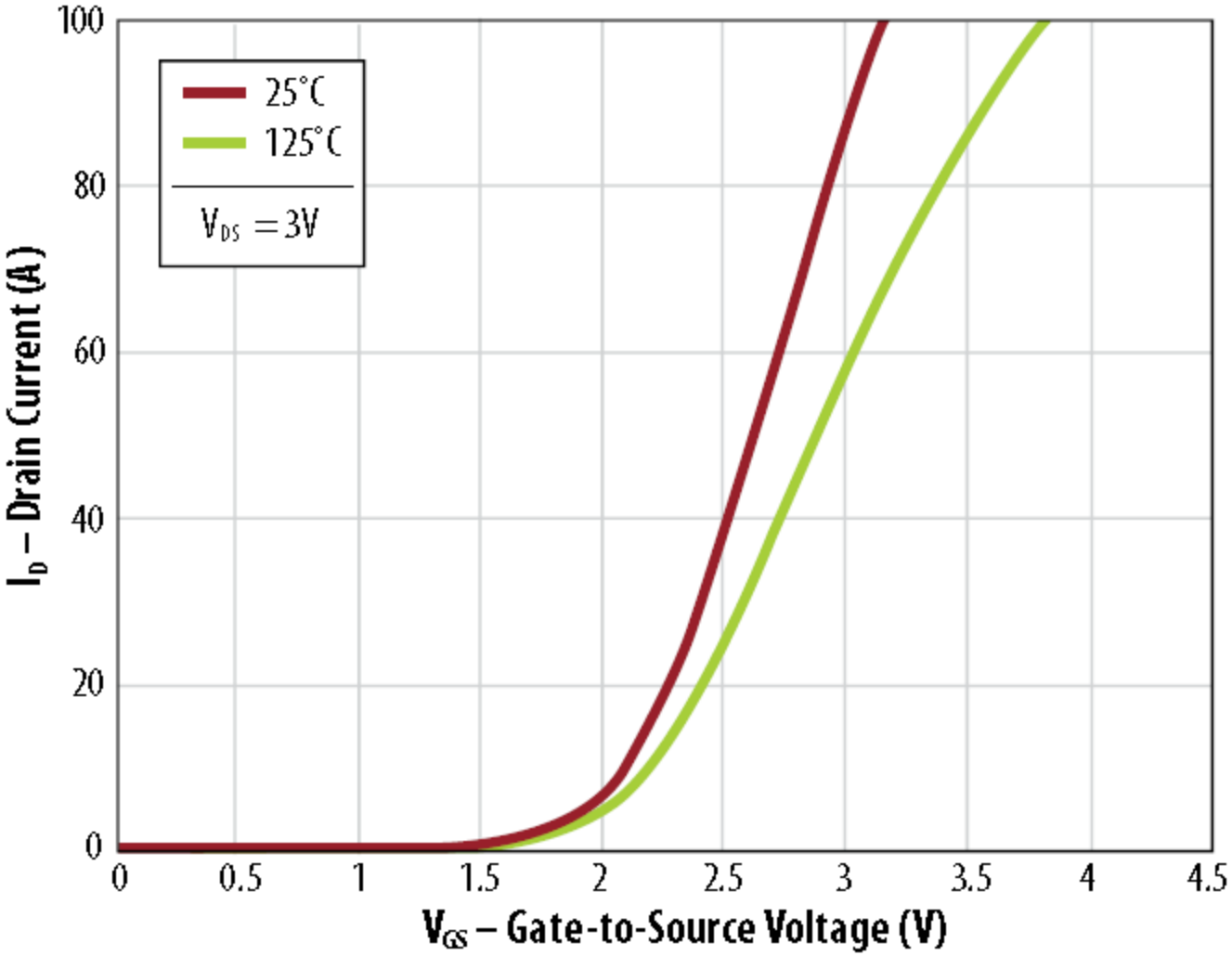
MOSFET Transfer Characteristics

Negative temperature coefficient region of silicon MOSFET

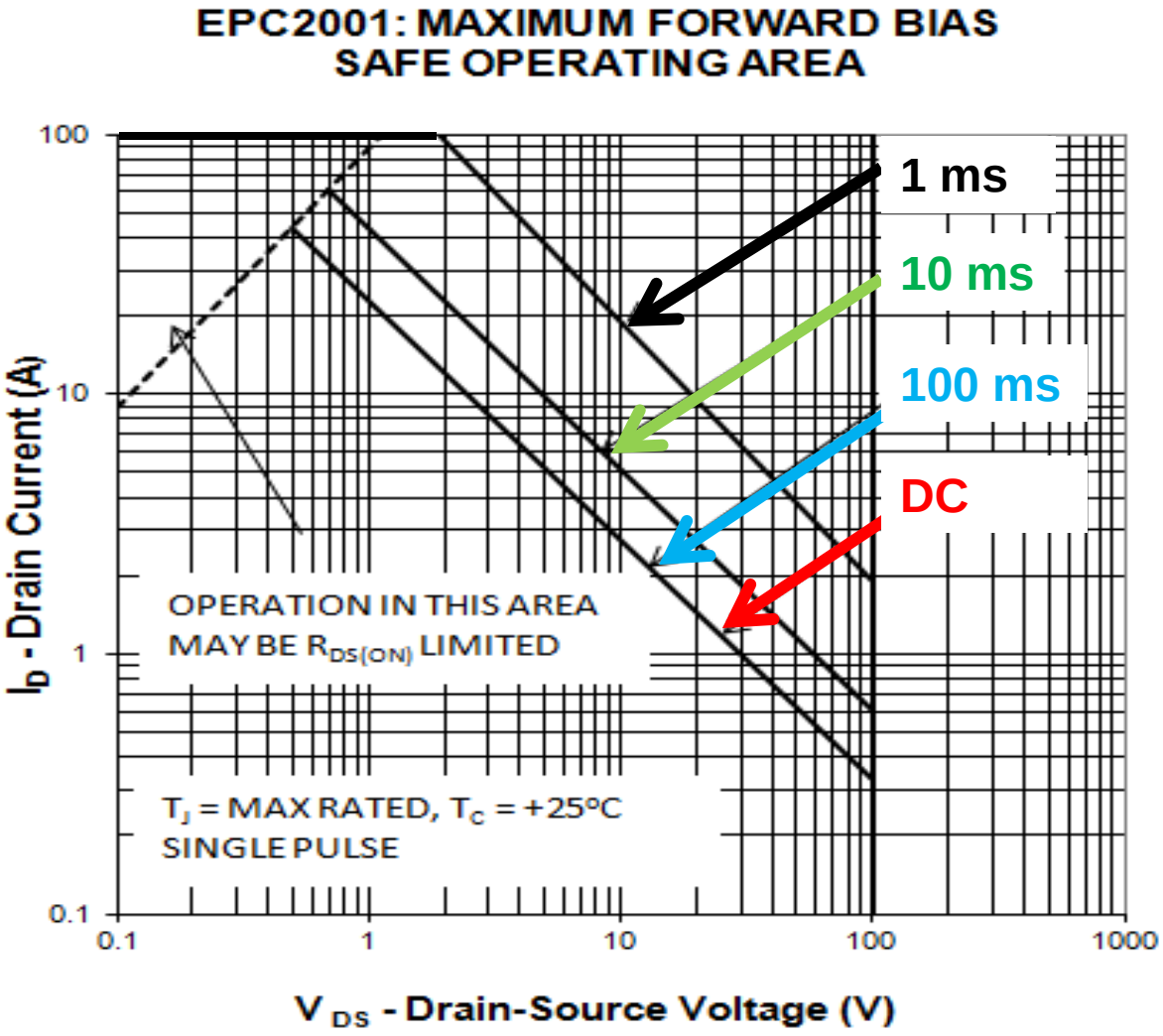


Source: www.infineon.com

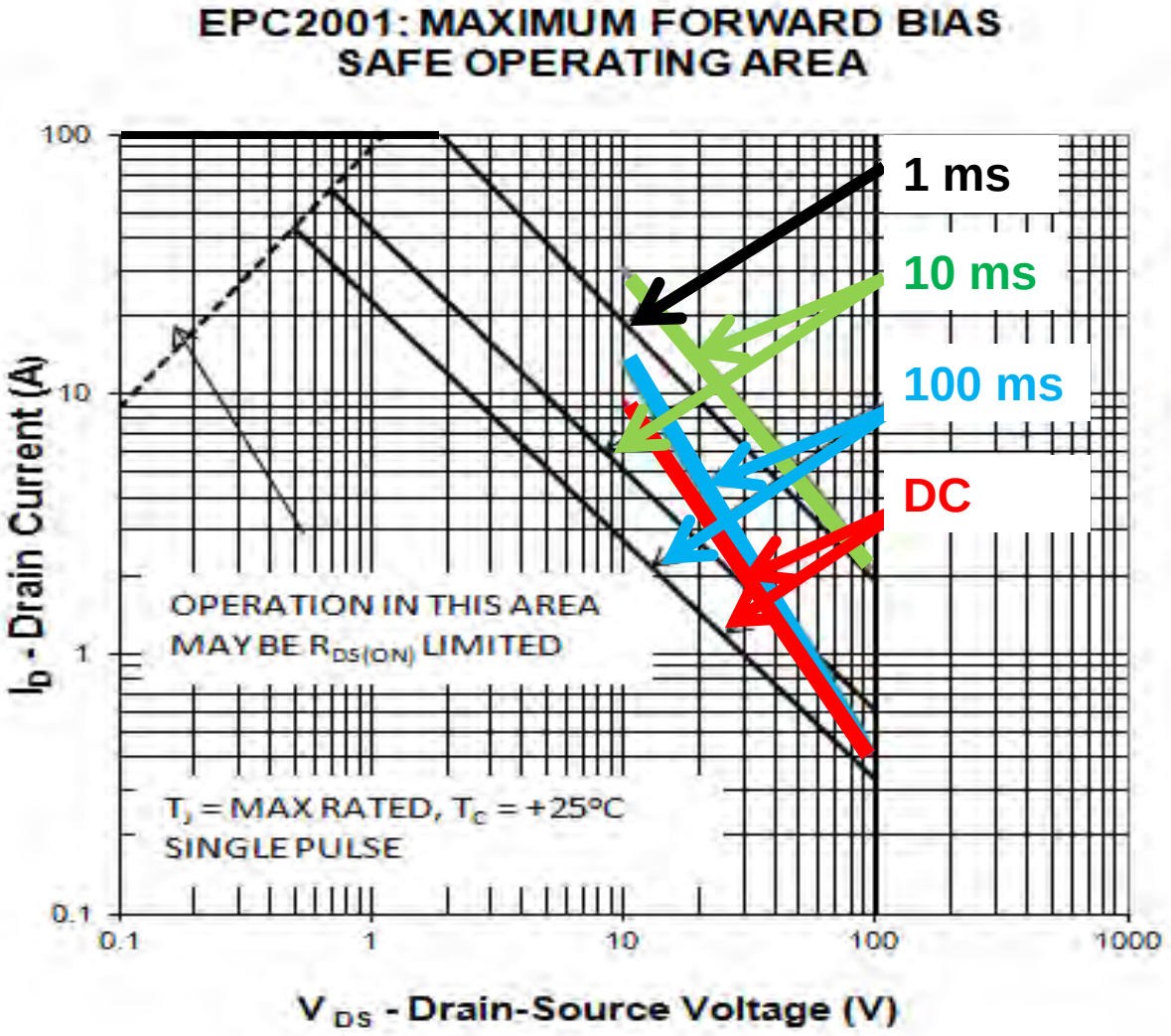
eGaN® FET Transfer Characteristics



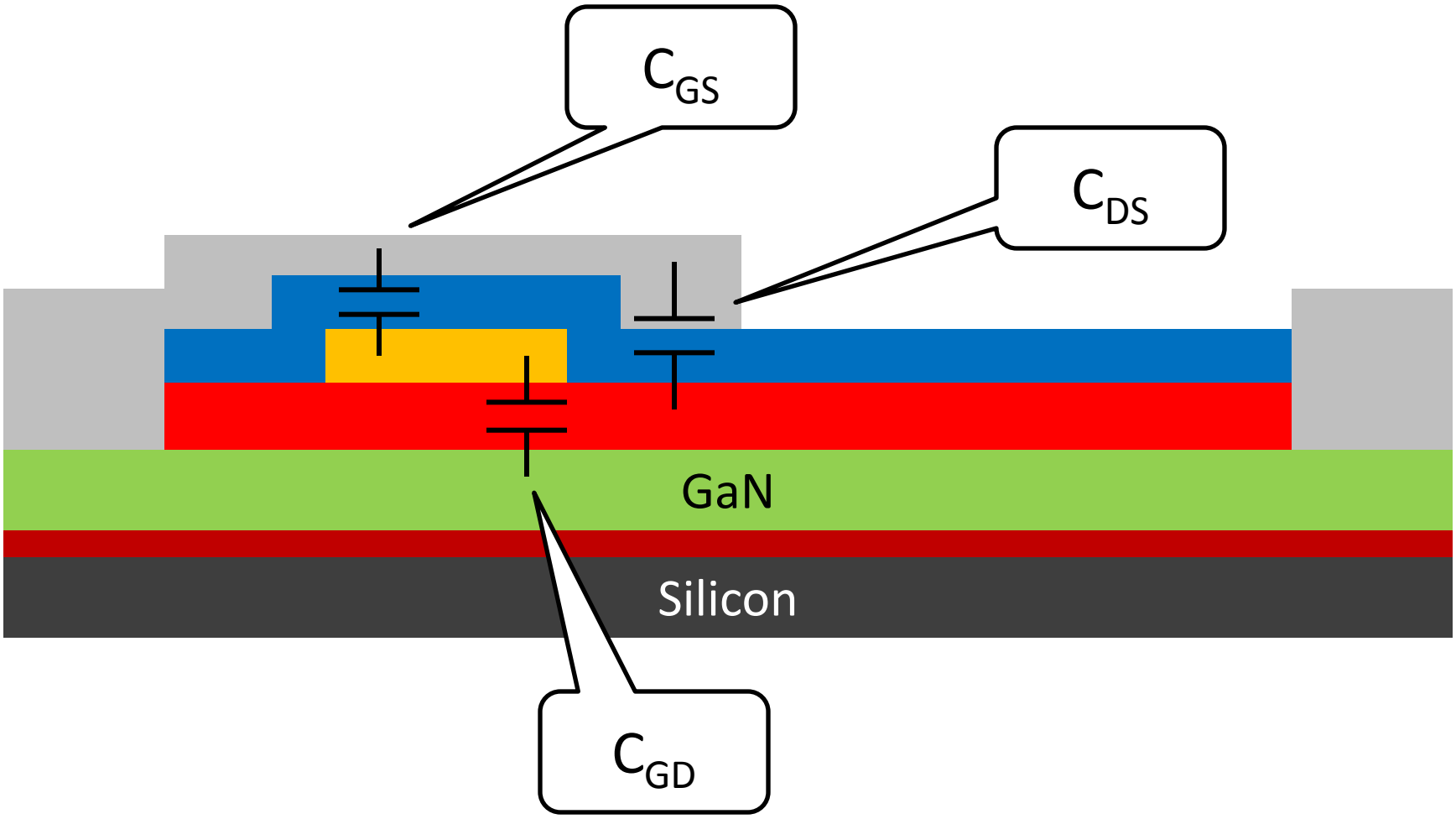
eGaN® FET Safe Operating Area



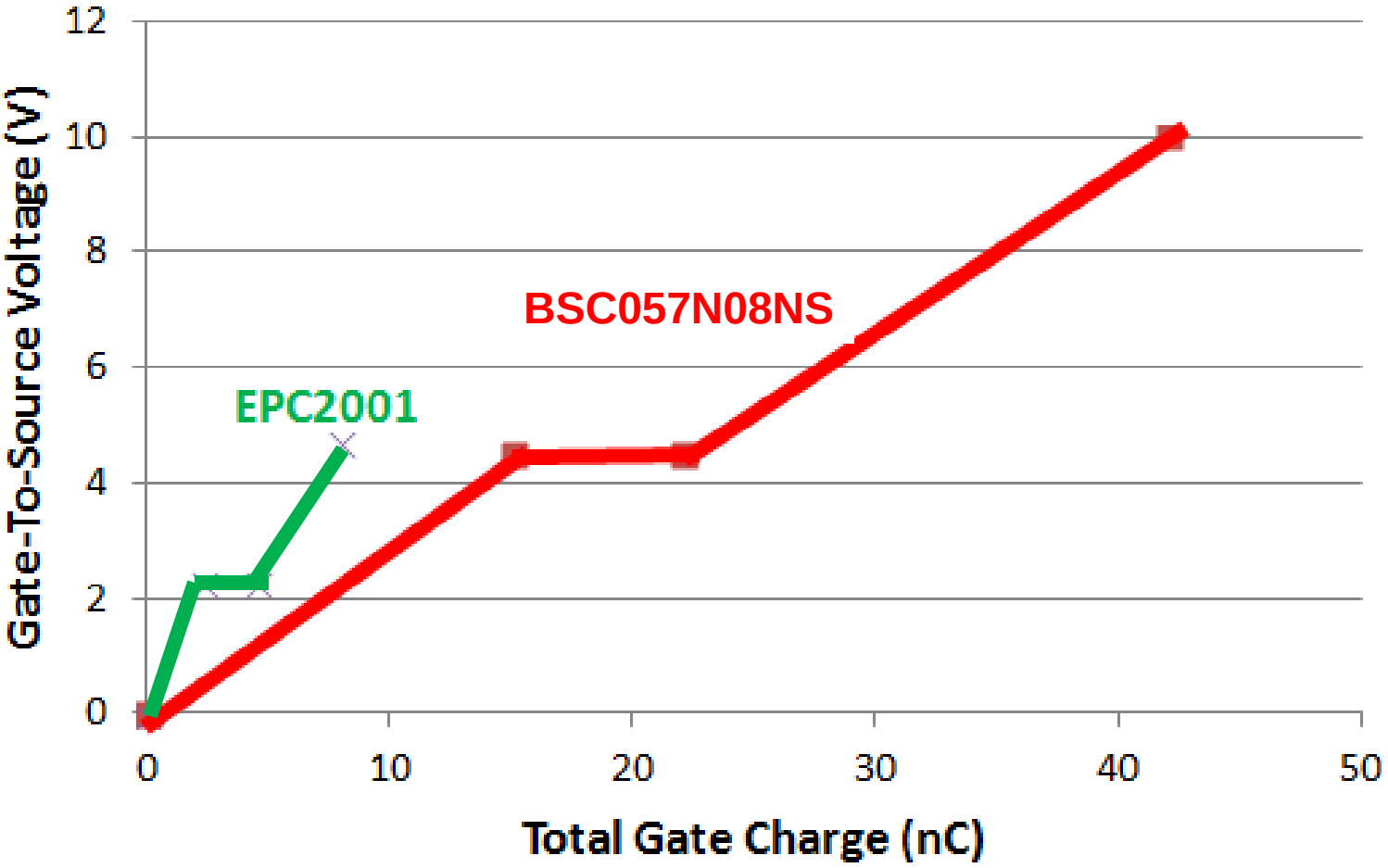
eGaN® FET Safe Operating Area



eGaN® FET Capacitances

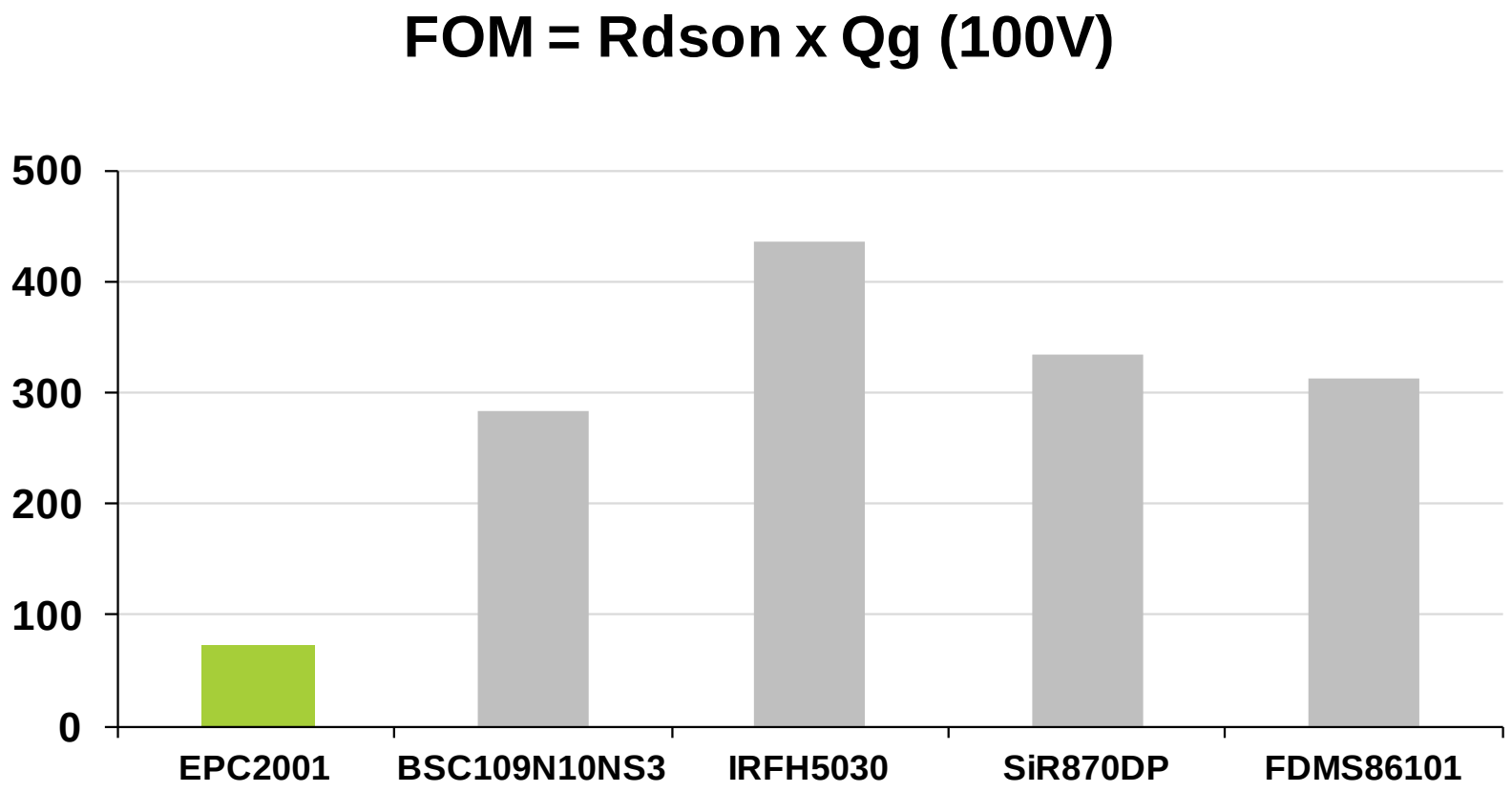


Total Gate Charge



EPC2001 = 100 V, 5.6 mΩ typ
BSC057N08 = 80 V, 4.7 mΩ typ

Figure of Merit



eGaN® FET Loss Mechanisms

Like A MOSFET

- I^2R Conduction Loss
- Capacitive Switching Losses
- Gate Drive Losses
- V×I Switching Loss

Not Like A MOSFET

- High Reverse Conduction Loss
- No Body Diode Reverse Recovery Loss

eGaN® FET Loss Mechanisms

Like A MOSFET

- I^2R Conduction Loss
- Capacitive Switching Losses
- Gate Drive Losses
- V×I Switching Loss

Not Like A MOSFET

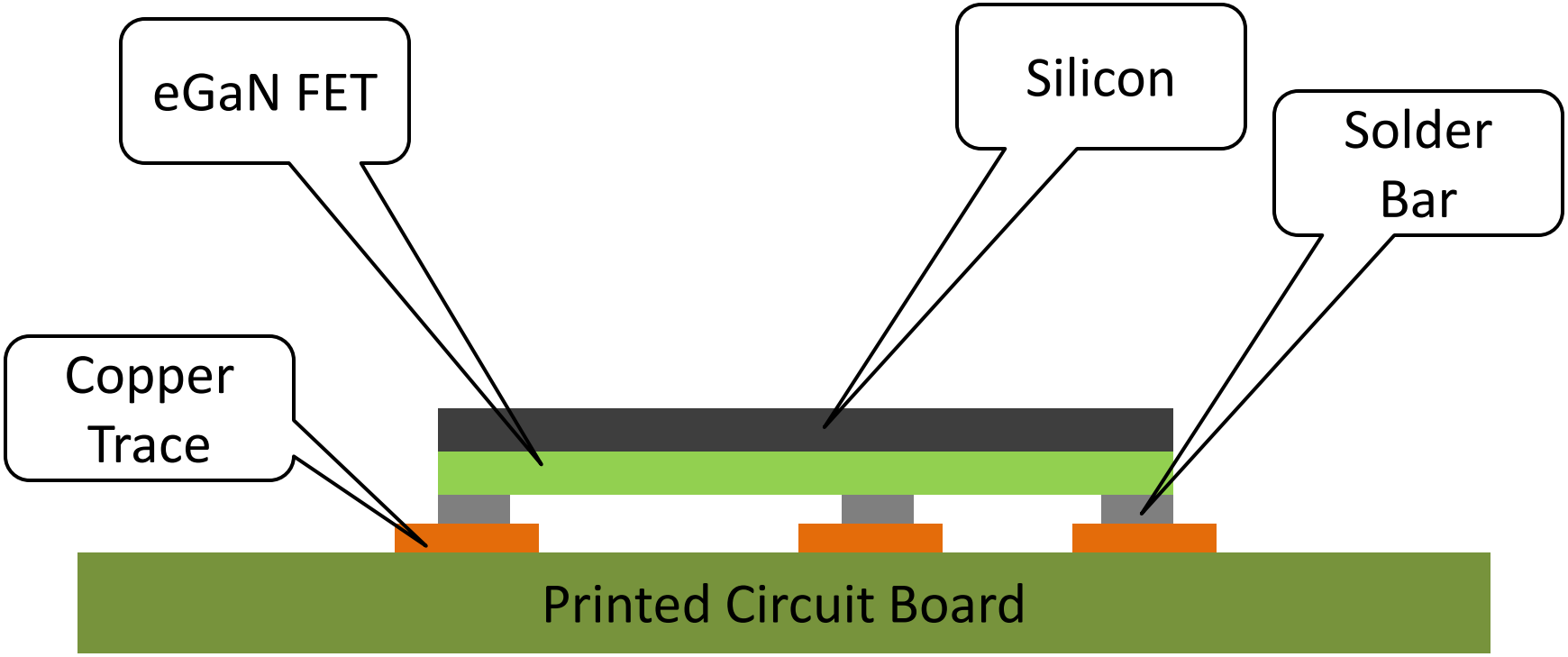
- High Reverse Conduction Loss
- No Body Diode Reverse Recovery Loss

Can be much, much better than comparable silicon MOSFET

Package Wish List

- Low parasitic resistance
- Low parasitic inductance
- Low thermal resistance
- Small size
- Low cost

Flip-Chip LGA Construction

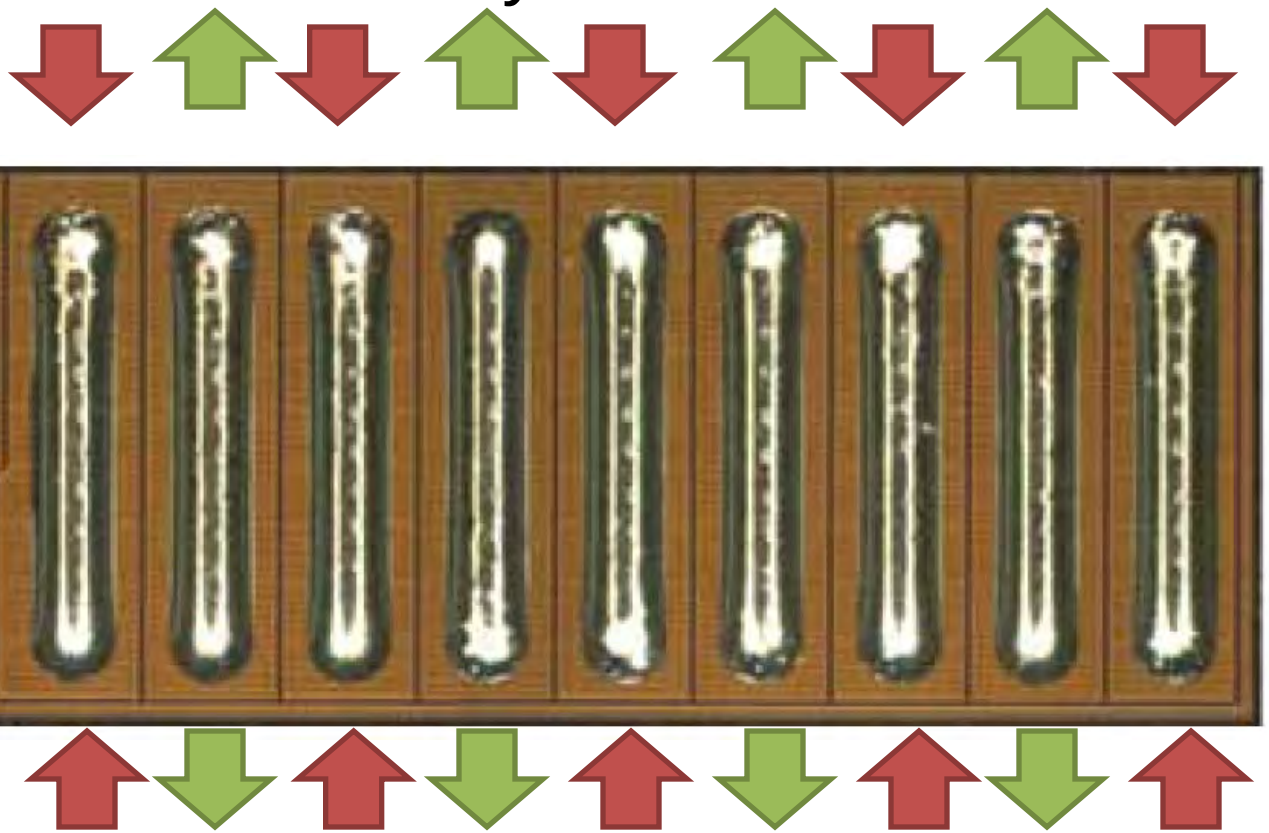


Absolute minimum
lead resistance and inductance!

LGA Construction

Drain Contacts

Interleaving to reduce layout inductance



Substrate

Gate

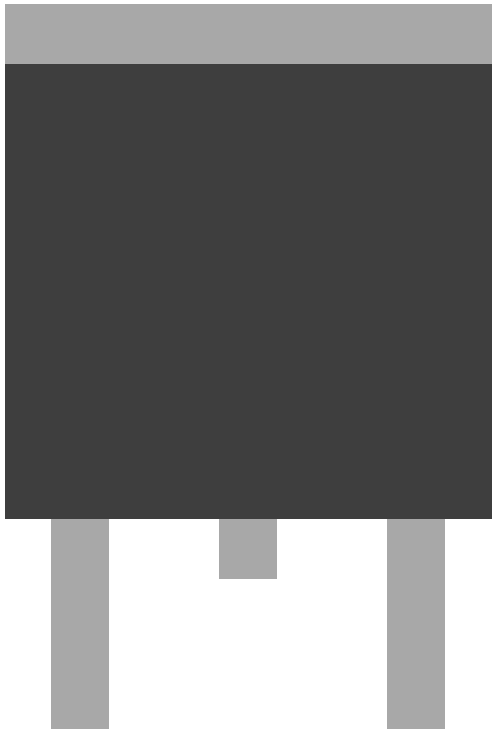
Source Contacts

Size Comparison – 200 V

D-PAK

eGaN FET

5.76 mm²



65.3 mm²

Drawn To Scale

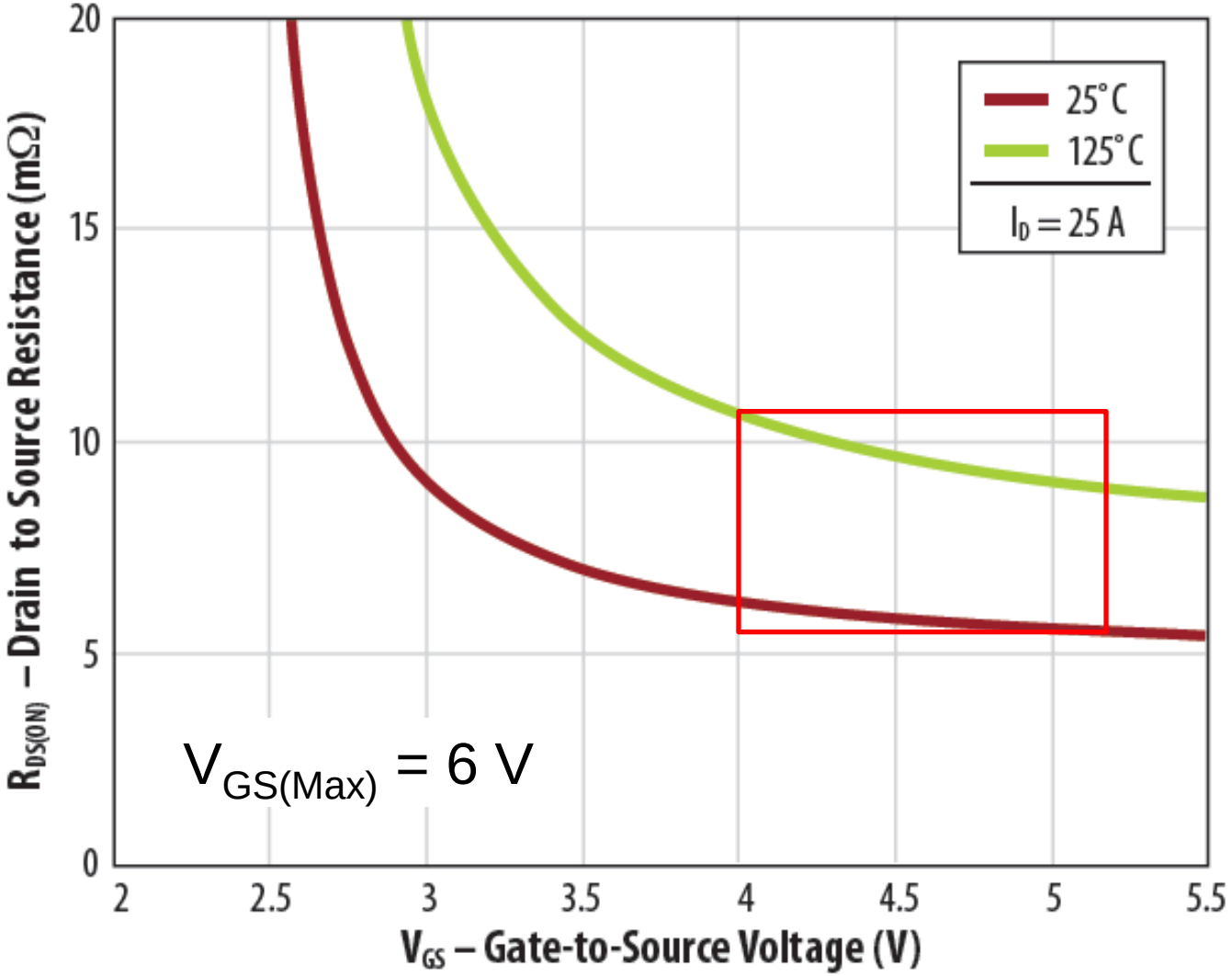
Key Applications

- Wireless Power Transmission – GaN Enabled
- RF DC-DC “Envelope Tracking” – GaN Enabled
- RadHard
- Power Over Ethernet
- RF Transmission
- Network and Server Power Supplies
- Point of Load Modules
- Energy Efficient Lighting
- Class D Audio

Design Basics Agenda

- Gate Driver Requirements
- Layout
- Thermal Management

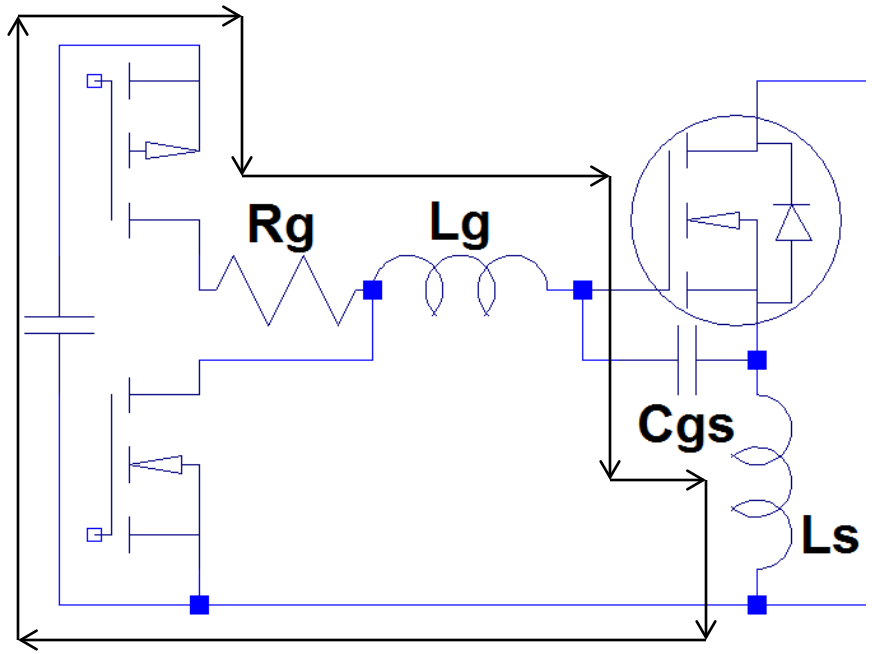
E-Mode Gate Drive - Low $V_{GS(ON)}$ Overhead



Gate Drive Solution

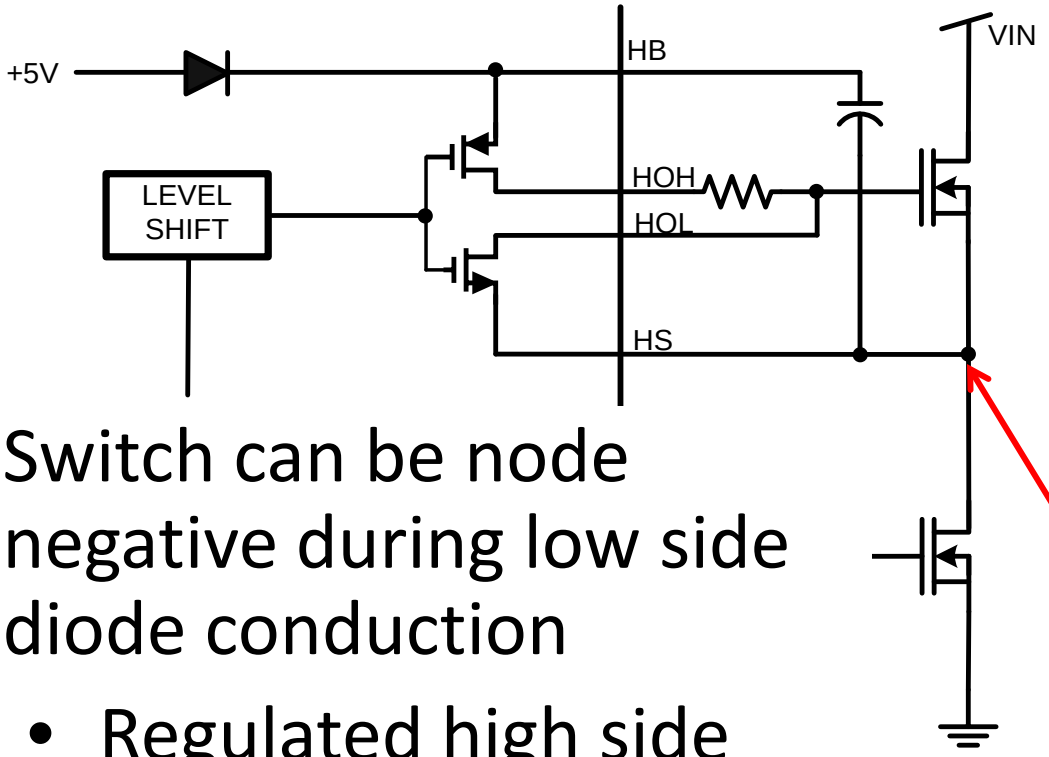
No overshoot:

$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$



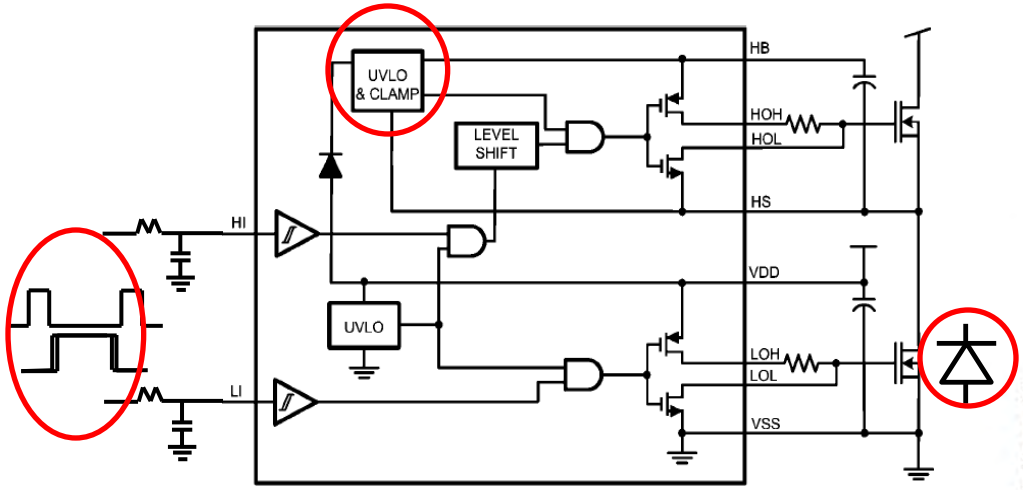
- Minimize inductance
  - Tight gate drive layout
  - BGA and LGA minimizes package inductance
  - Choose correct resistance
- Separate source and sink transistors allowing for separate drive paths.

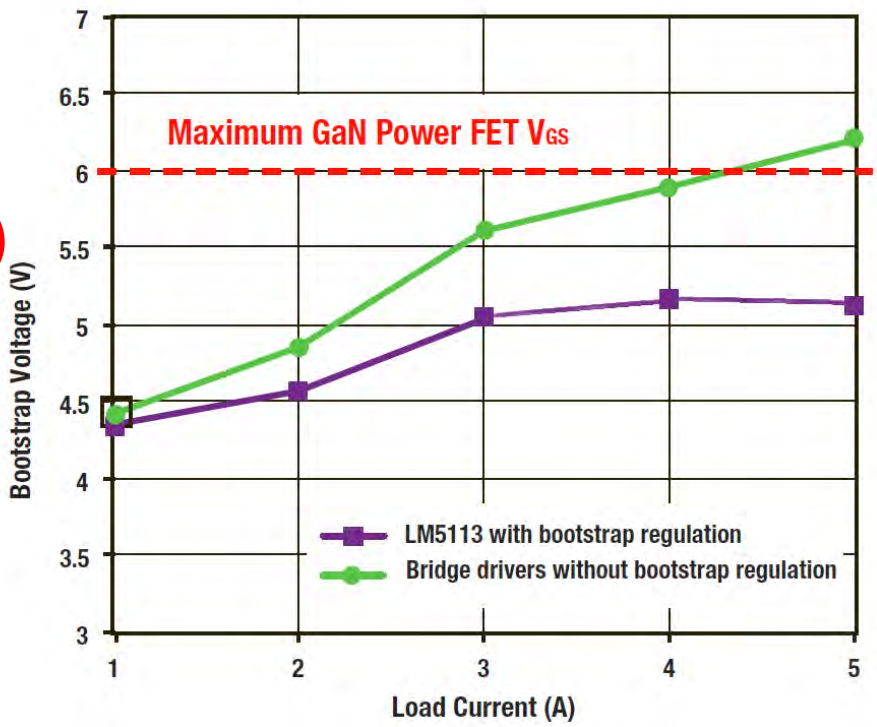
Bootstrap Supply



- Switch can be node negative during low side diode conduction
  - Regulated high side supply
  - Minimal dead time and slow bootstrap

High Side Regulation – LM5113



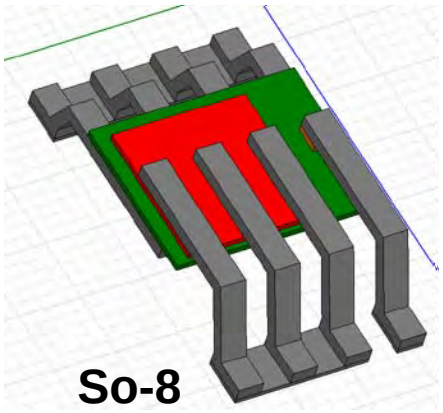


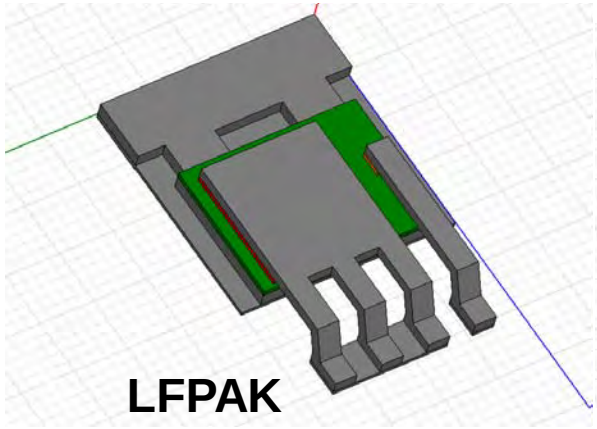
- Bootstrap clamp limits floating (HS) power supply
- Separate control inputs allow accurate, flexible tuning to minimize dead-time
- Well matched channel-to-channel propagation delays are critical
- Optional Schottky in parallel

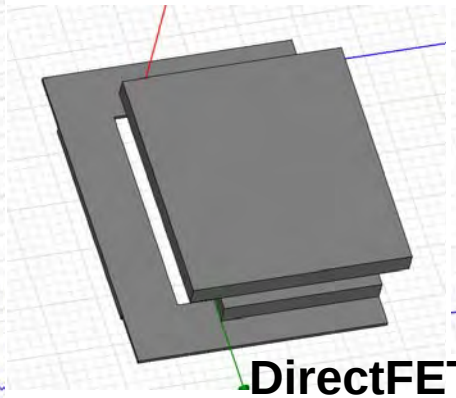
Texas Instruments, "Gate Drivers for Enhancement Mode GaN Power FETs 100 V Half-Bridge and Low-Side Drivers Enable Greater Efficiency, Power Density, and Simplicity", SNVB001

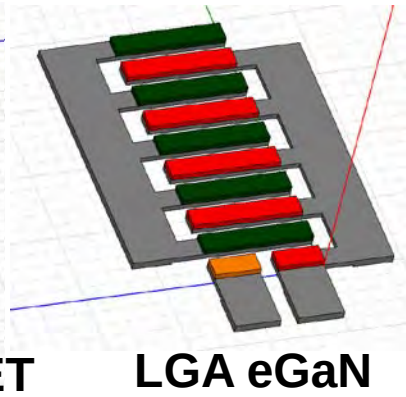
Layout

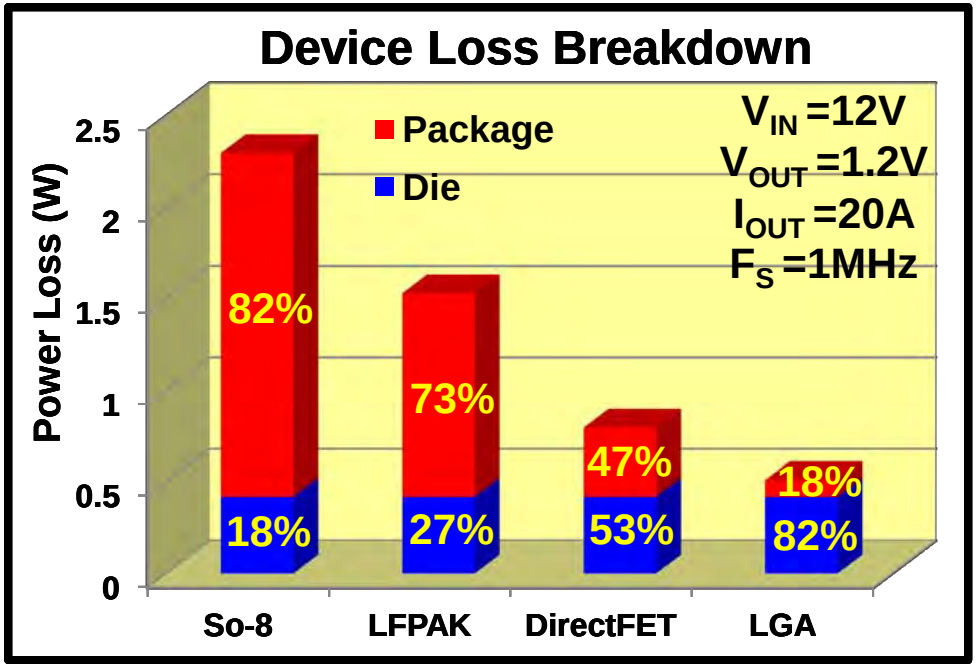
Packaging Evolution

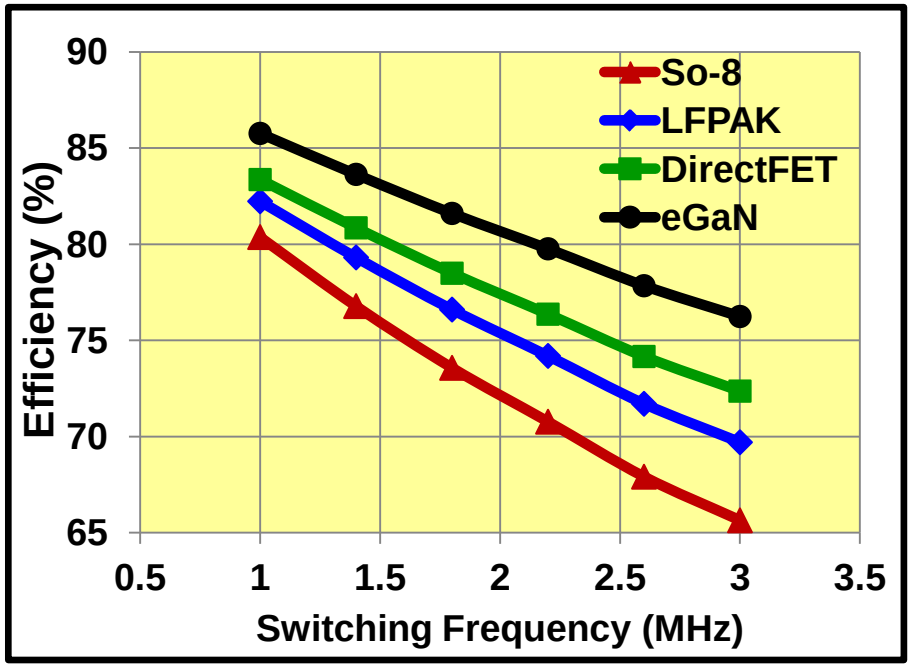




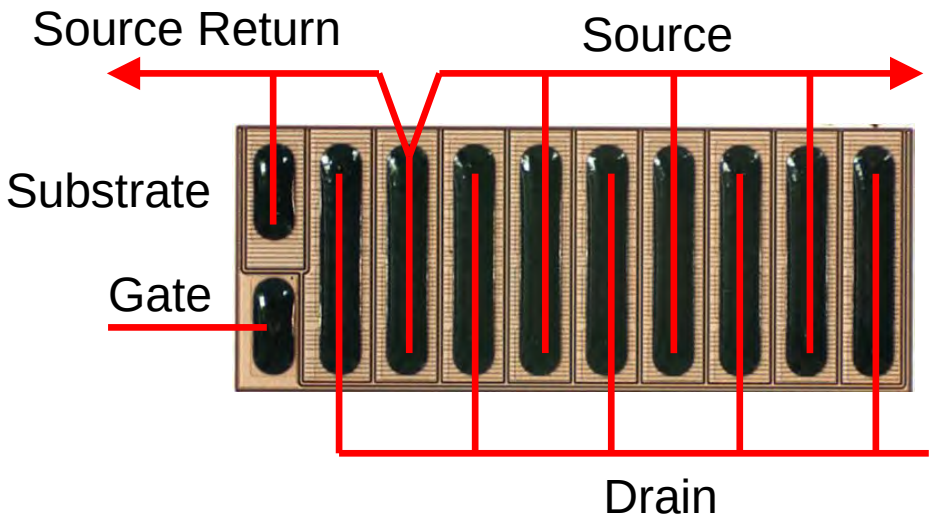


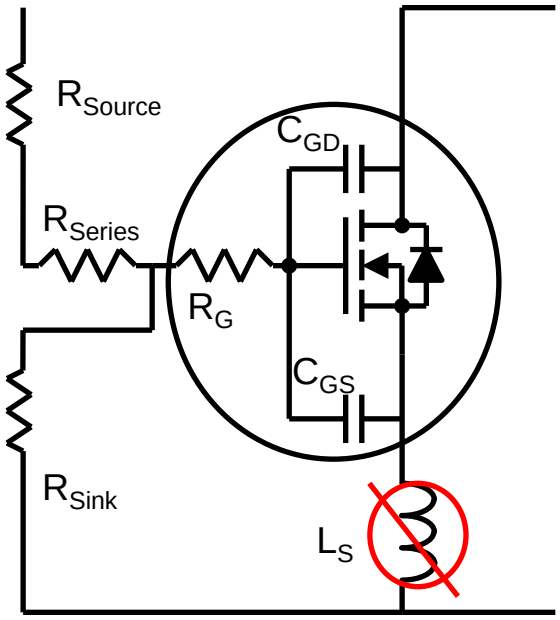






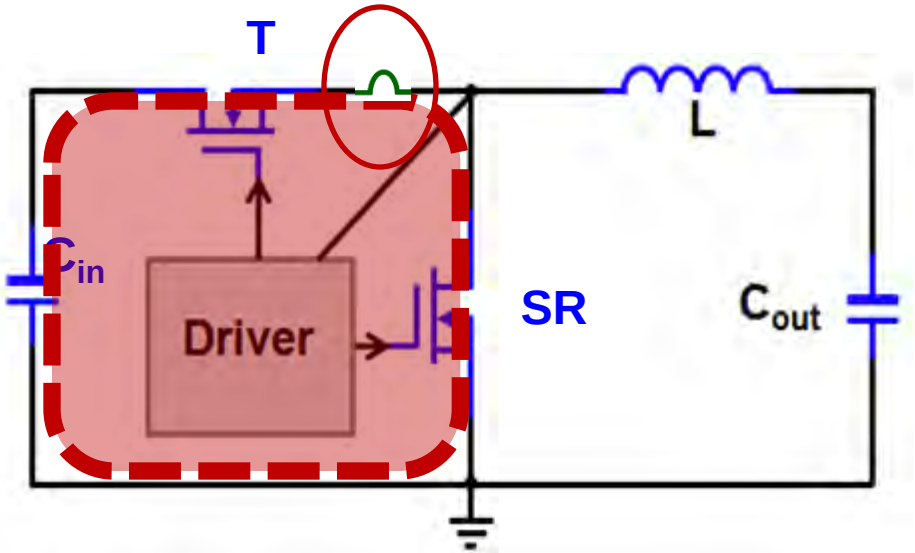
Generating Kelvin Source Connection





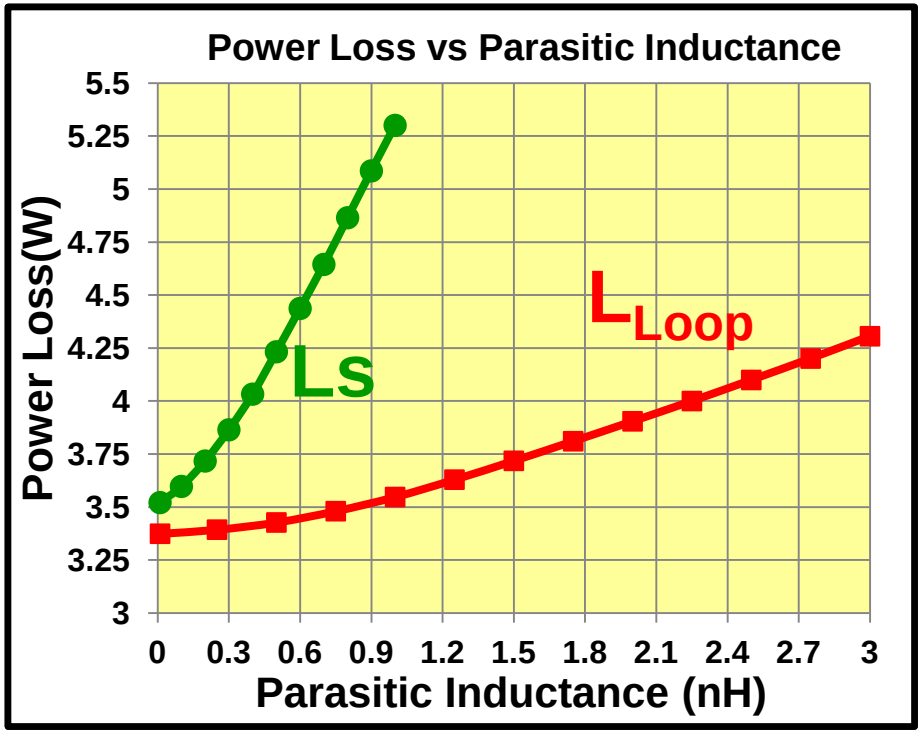
Minimize Common Source Inductance

Buck Converter Parasitics



L_S: Common Source Inductance

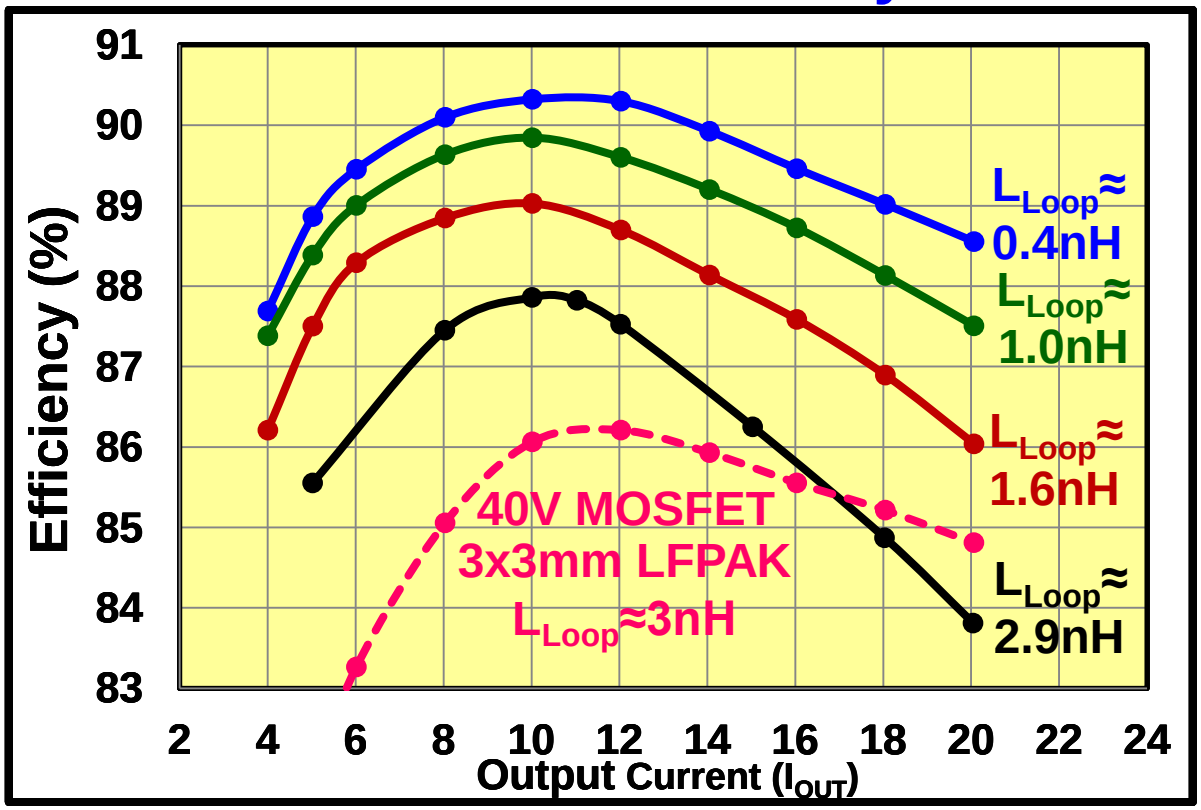
L_{Loop}: High Frequency Power Loop Inductance



V_{IN}=12 V, V_{OUT}=1.2 V,
F_S=1 MHz, I_{OUT}= 20 A

Layout Impact on Efficiency

Measured Efficiency



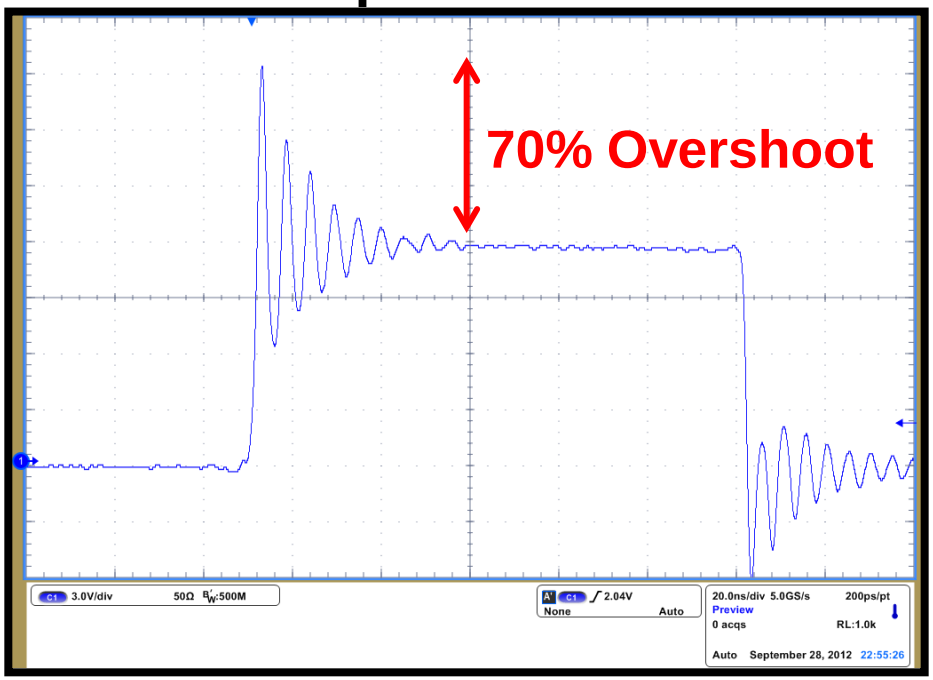
Experimental Prototype

L_{LOOP}≈0.4 nH

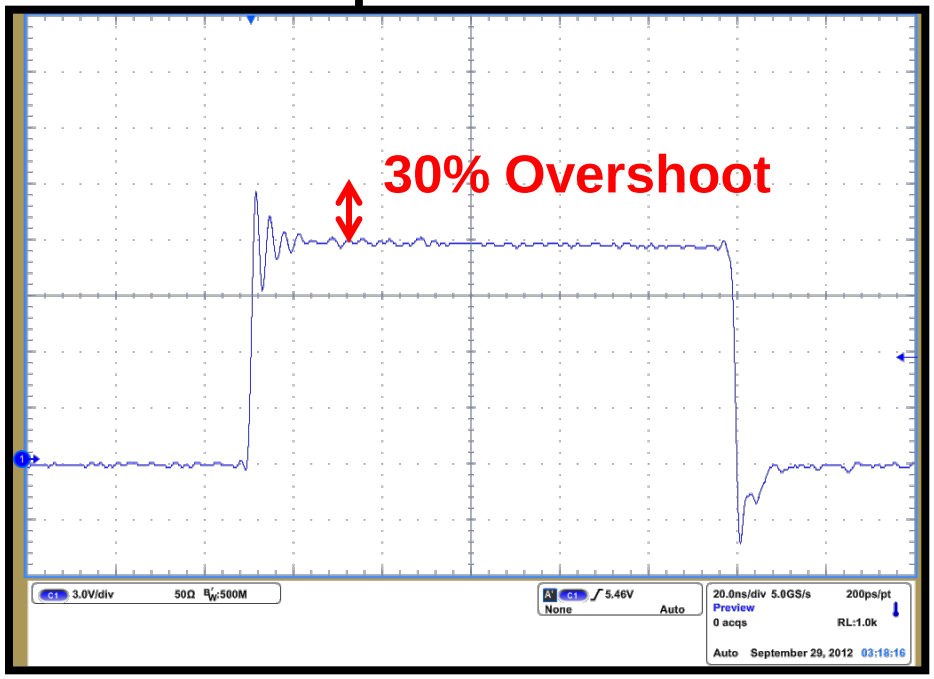
V_{IN}=12 V, V_{OUT}=1.2 V,
F_S=1 MHz, L=150 nH

Layout Impact on Peak Voltage

L_{Loop}≈1.0 nH



L_{Loop} ≈ 0.4 nH



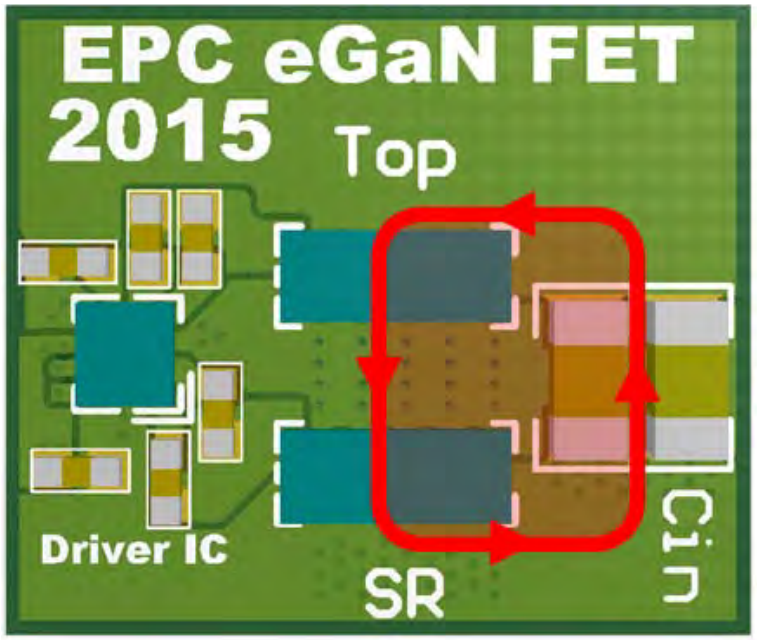
Switching Node Voltage

V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A

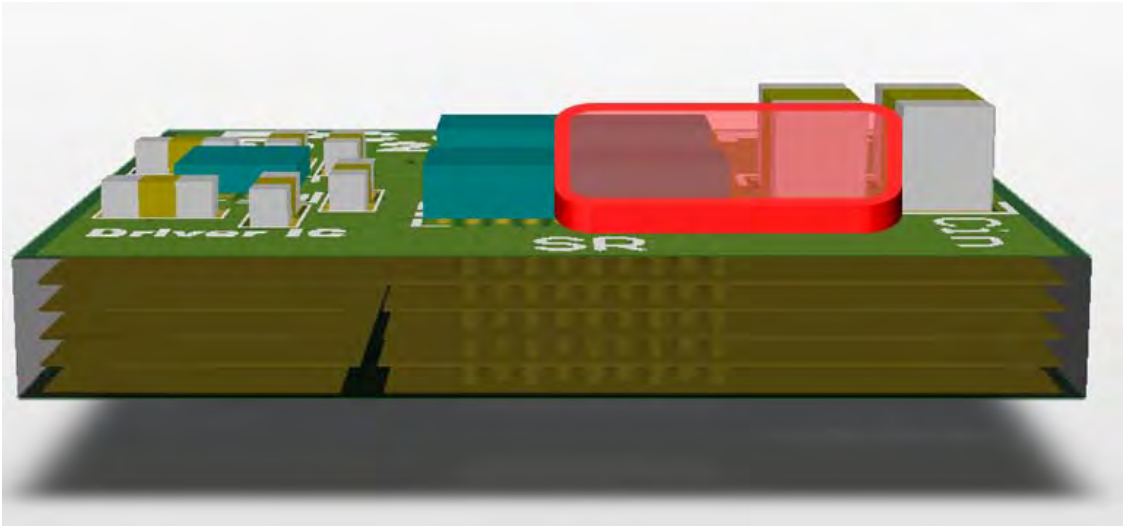
F_S=1 MHz L=150 nH

Conventional Lateral Layout

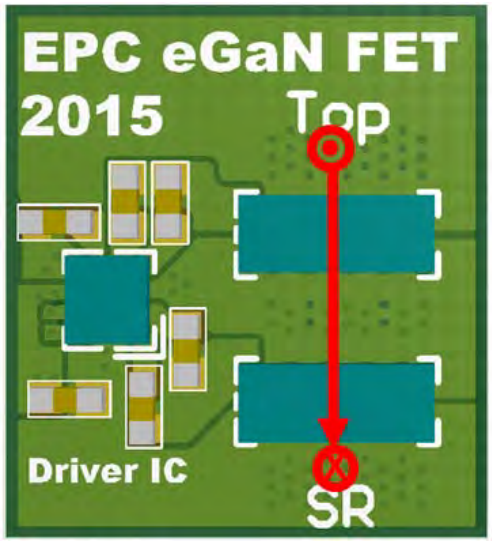
Top View



Side View

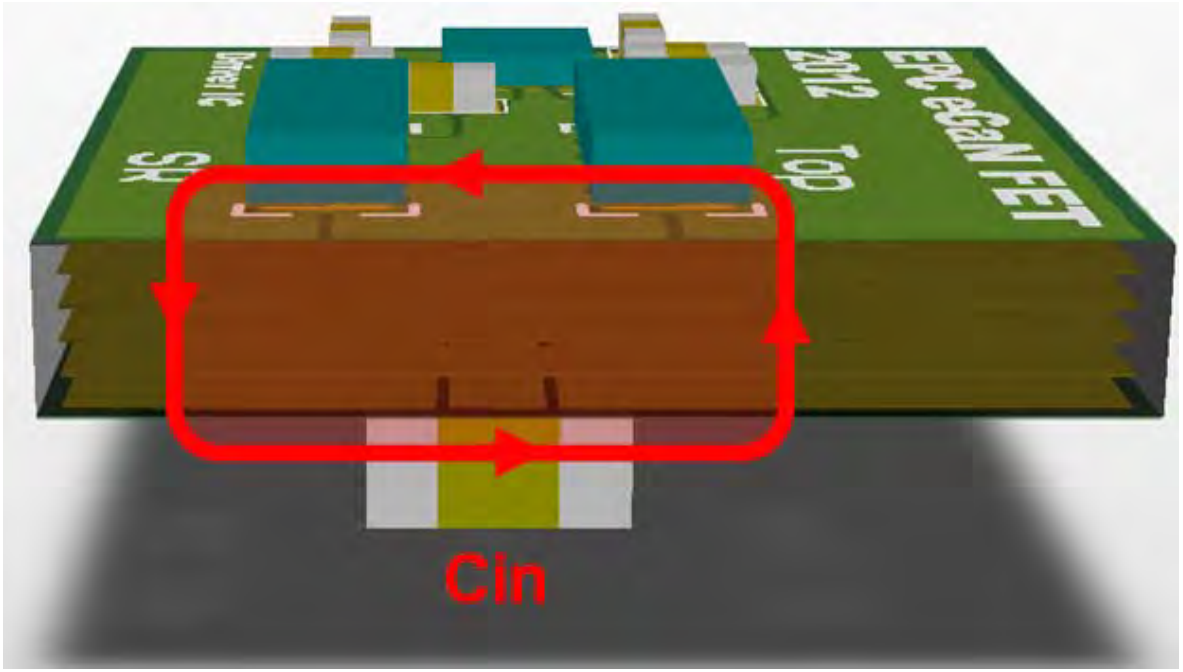


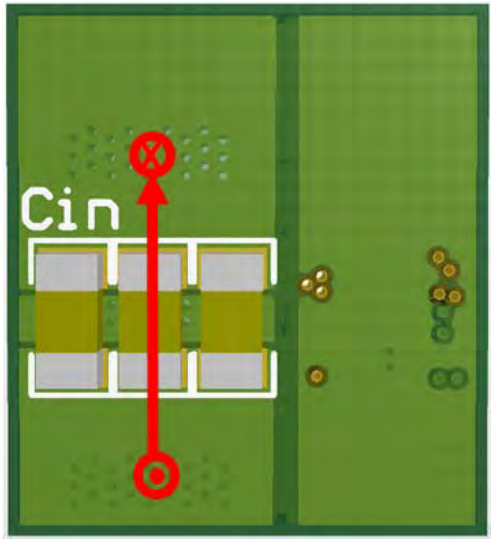
Conventional Vertical Layout



Top View

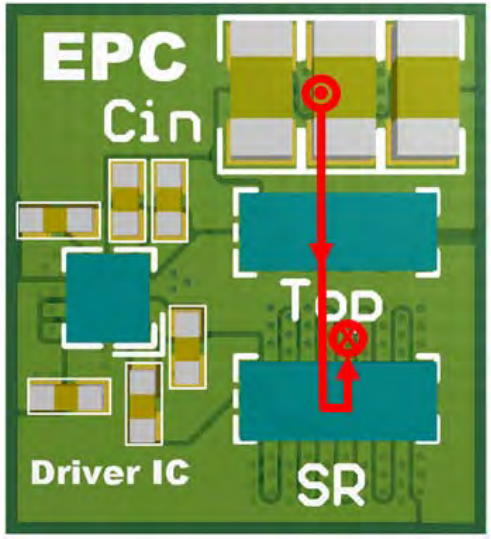
Side View





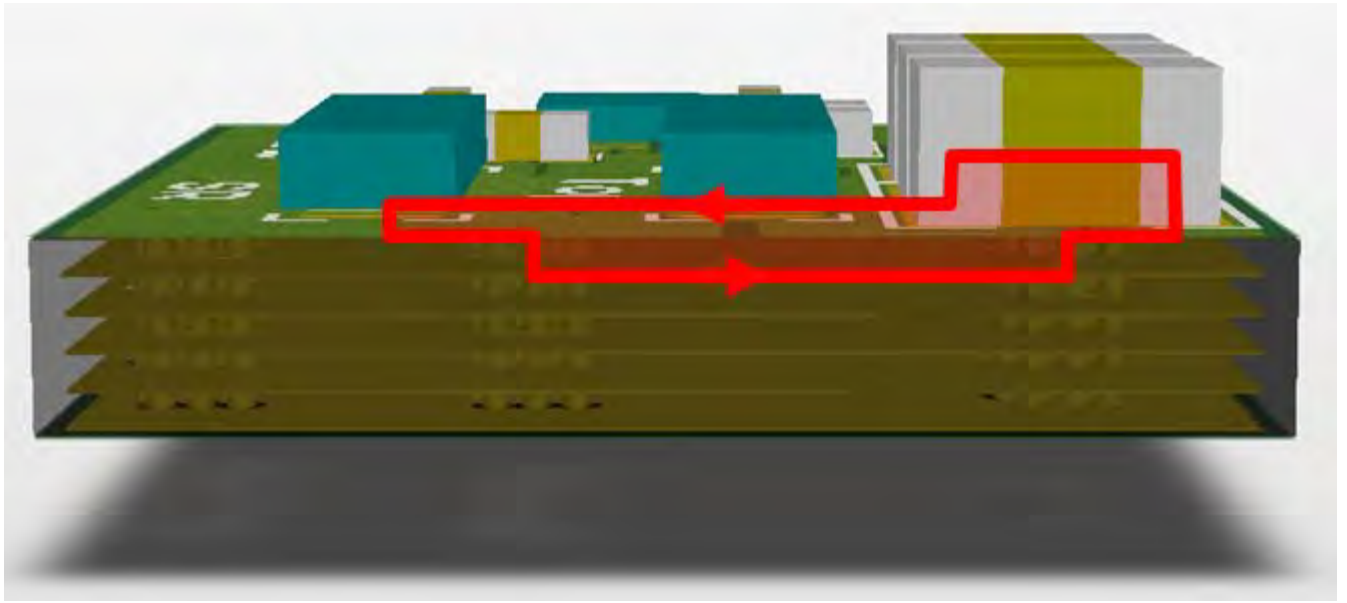
Bottom View

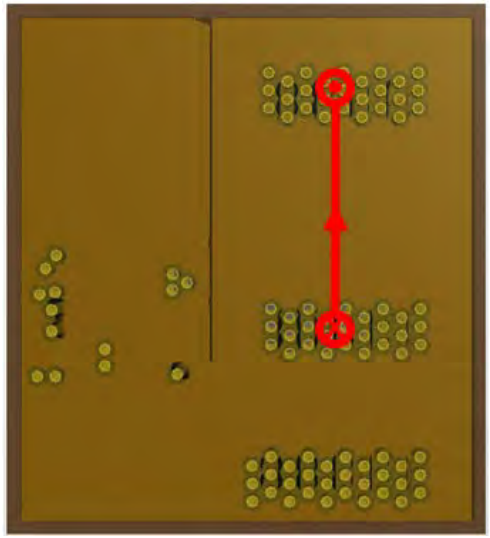
Optimal Layout



Top View

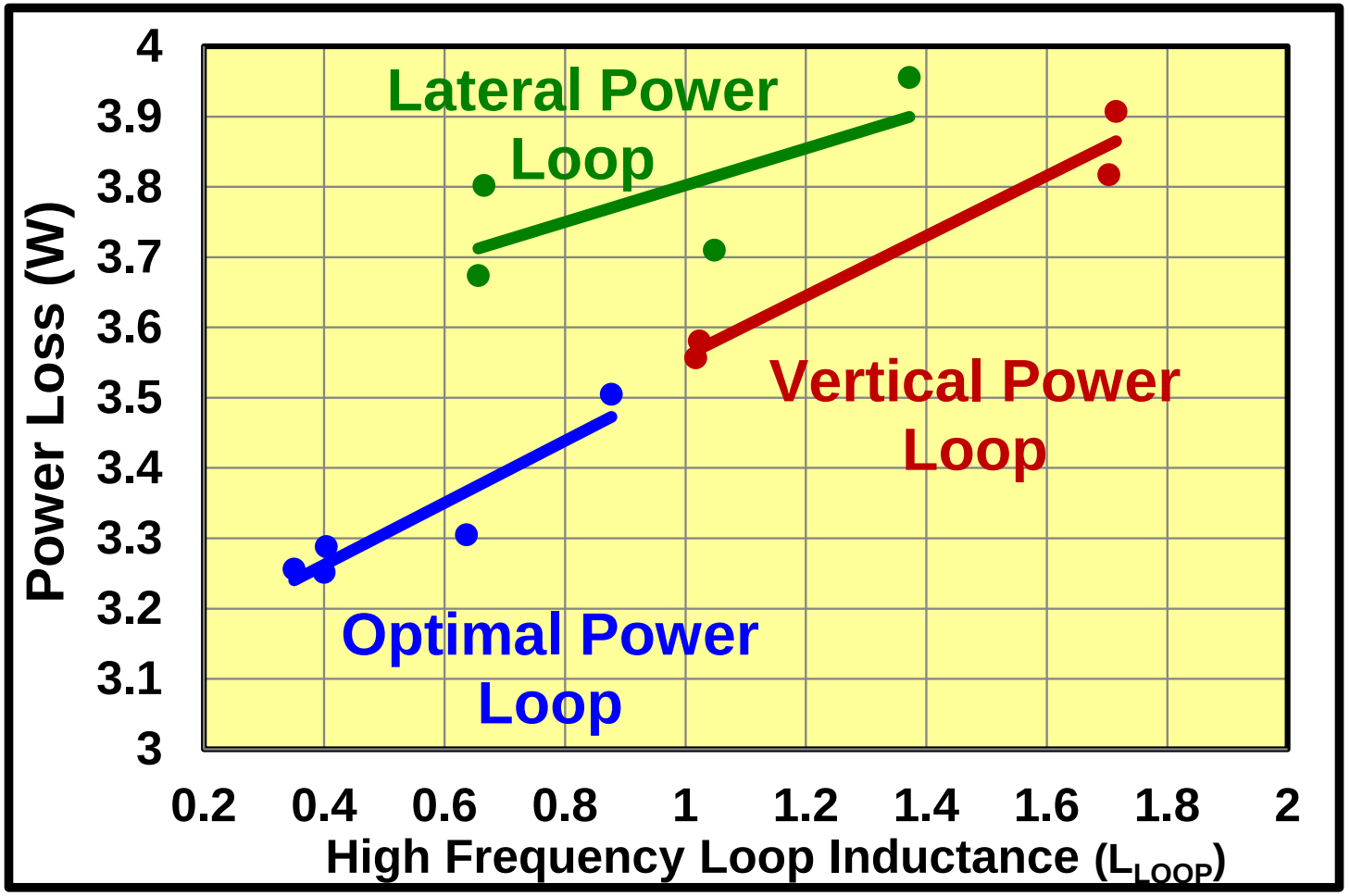
Side View





Top View
Inner Layer 1

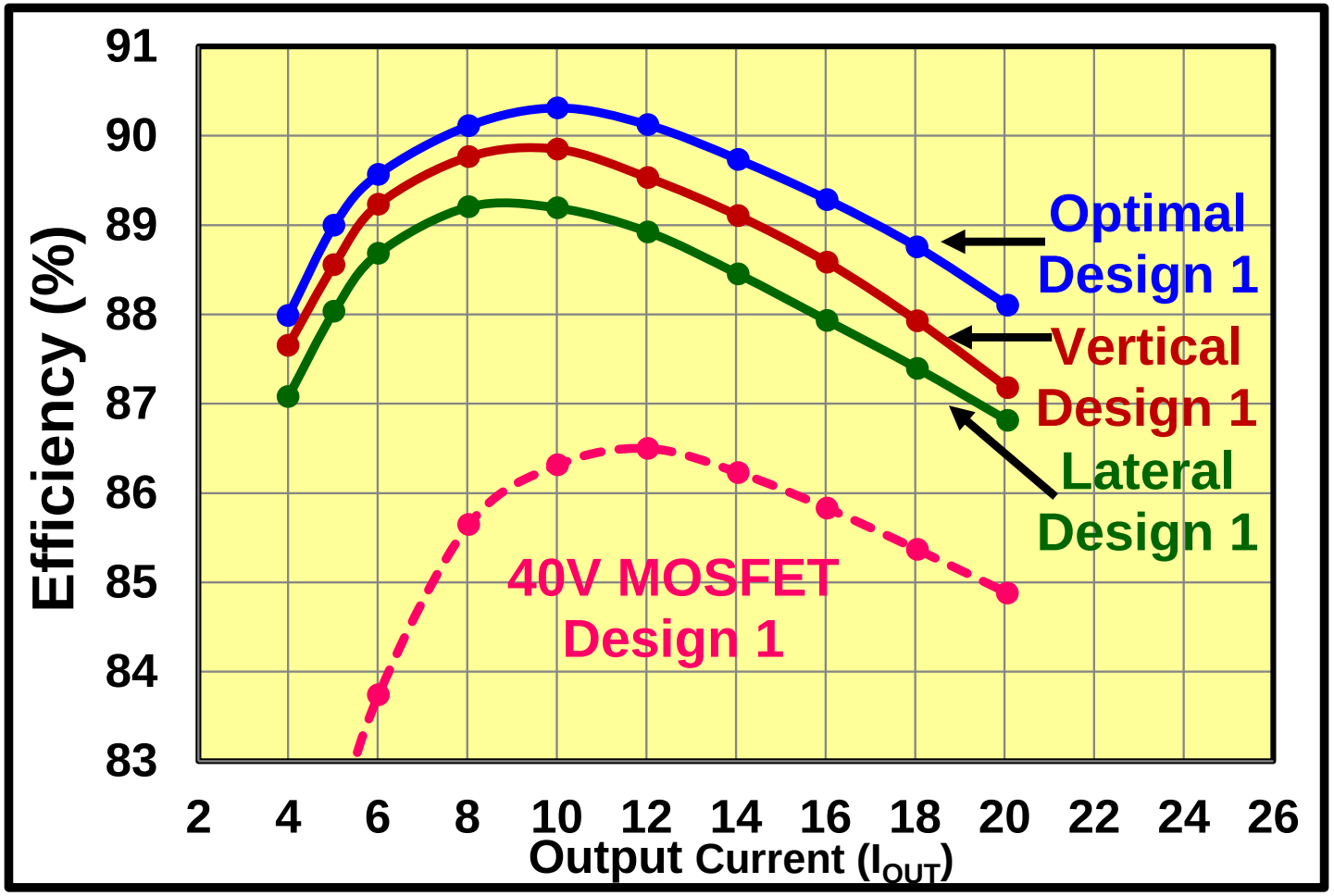
Power Loss Comparison



V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A F_S=1 MHz L=300 nH

T/SR: EPC2015 Driver LM5113

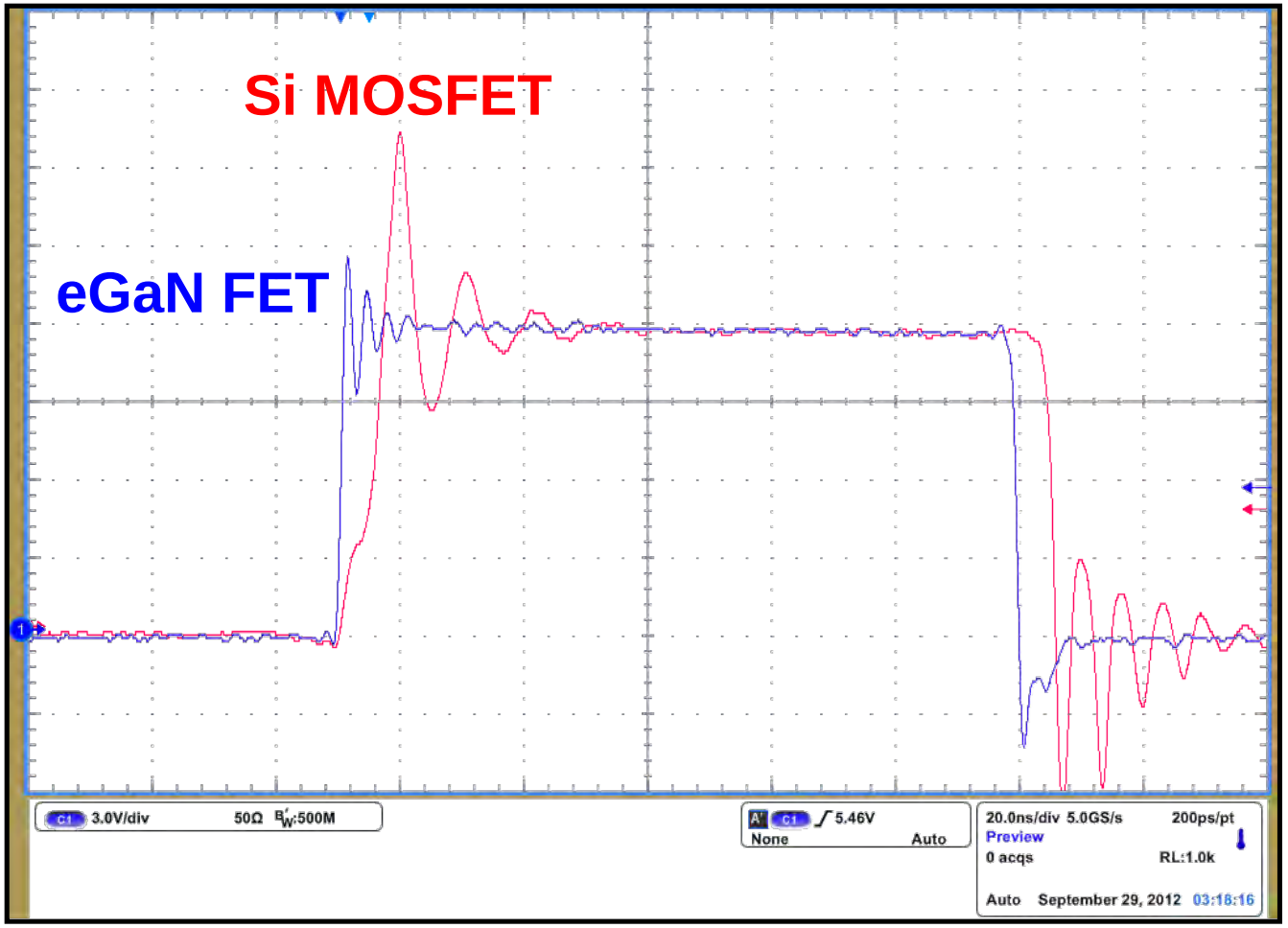
Efficiency Comparison



V_{IN}=12 V V_{OUT}=1.2 V F_S=1 MHz L=300 nH

T/SR: EPC2015 Driver LM5113

eGaN® FET vs. MOSFET



V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A F_S=1 MHz L=300 nH eGaN FET T/SR: EPC2015 MOSFET T:BSZ097N04LS SR:BSZ040N04LS

Layout Summary

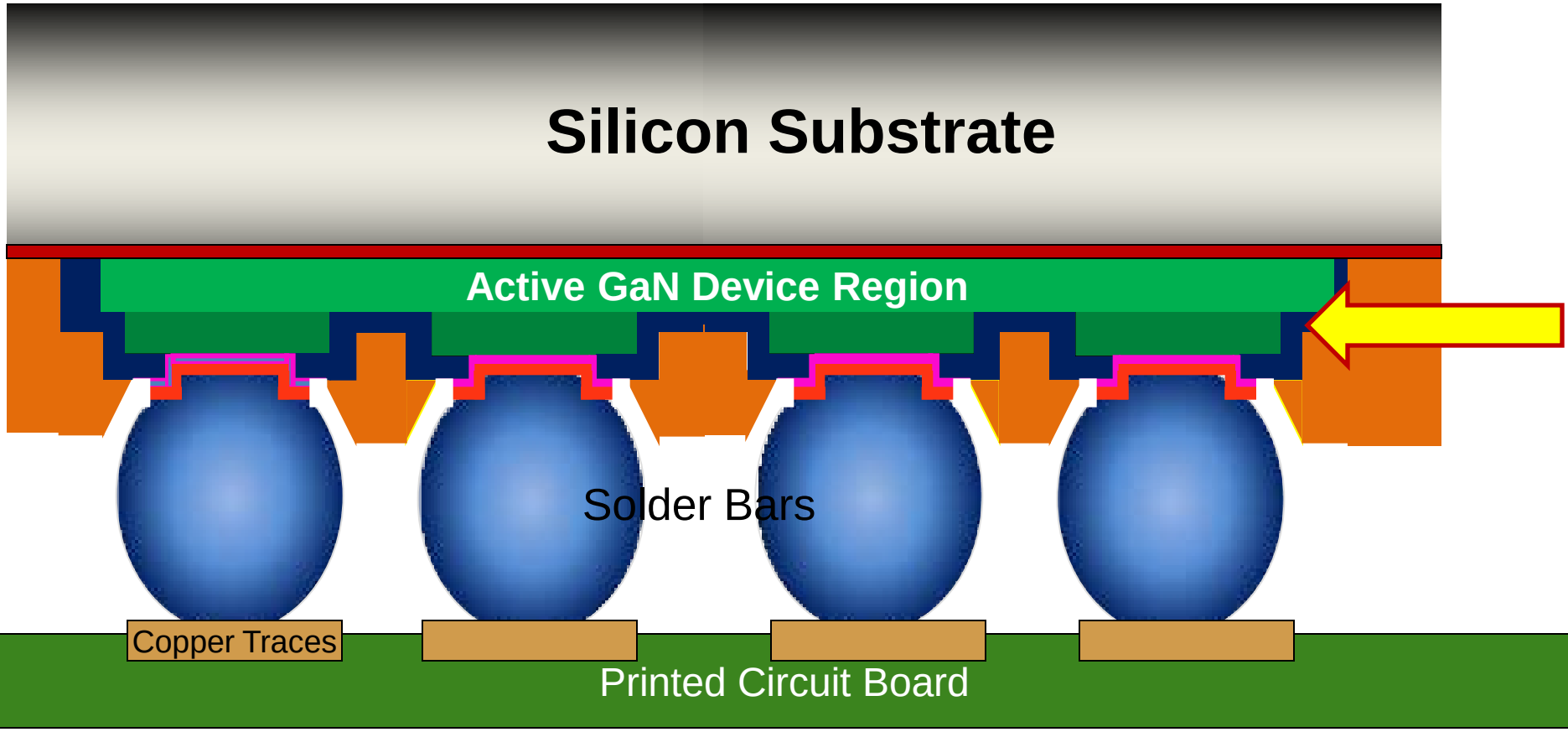
eGaN FETs improve performance in high switching frequency converters

- CSI is a critical component for maximizing switching performance
- Gate drive loop inductance limits switching speed
- Optimizing power loop inductance improves efficiency and minimizes voltage overshoot
- Current measurements affect performance
- Voltage measurements are bandwidth limited
- Reduced ringing reduces EMI

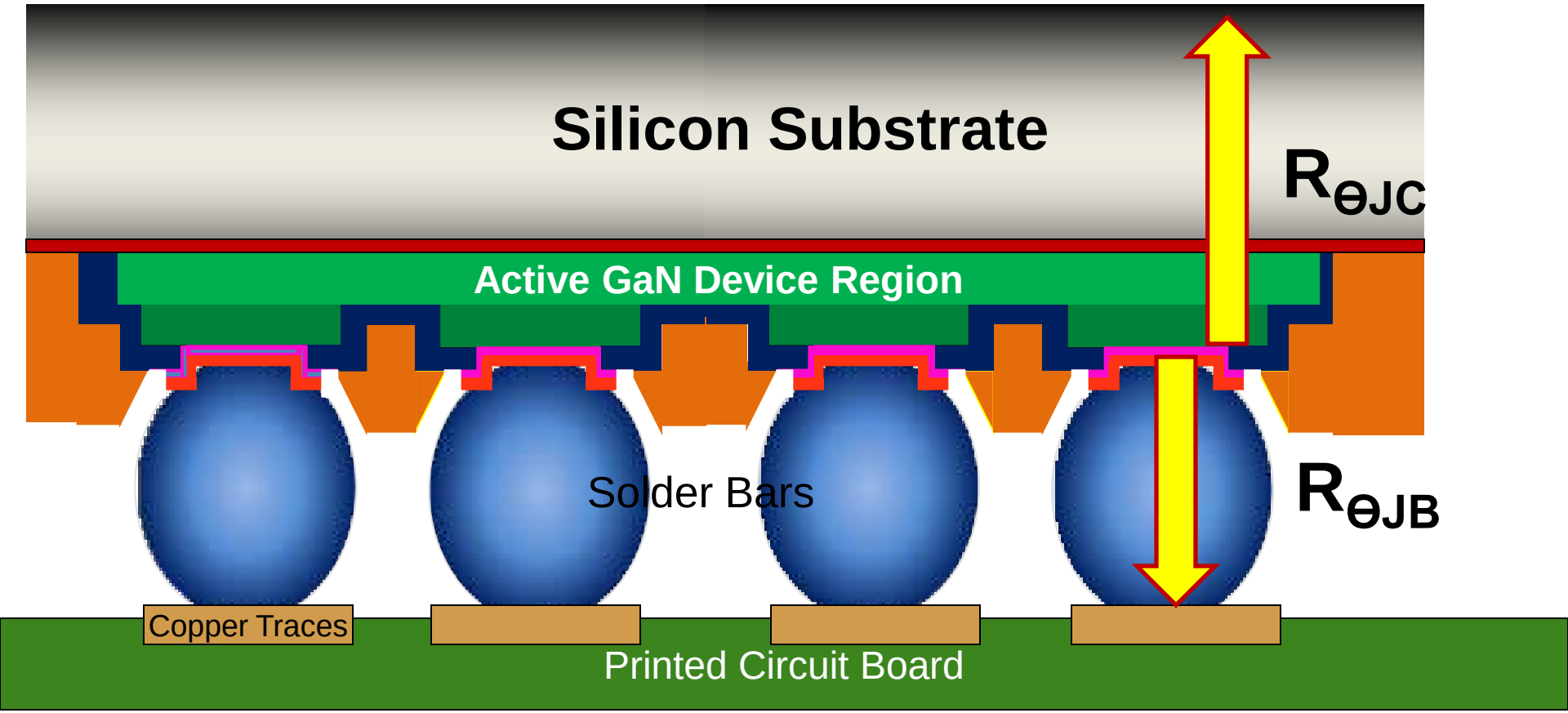
Thermal Management

Thermal Management

Heat Is Generated In GaN Material
Essentially On The Surface Of The Die

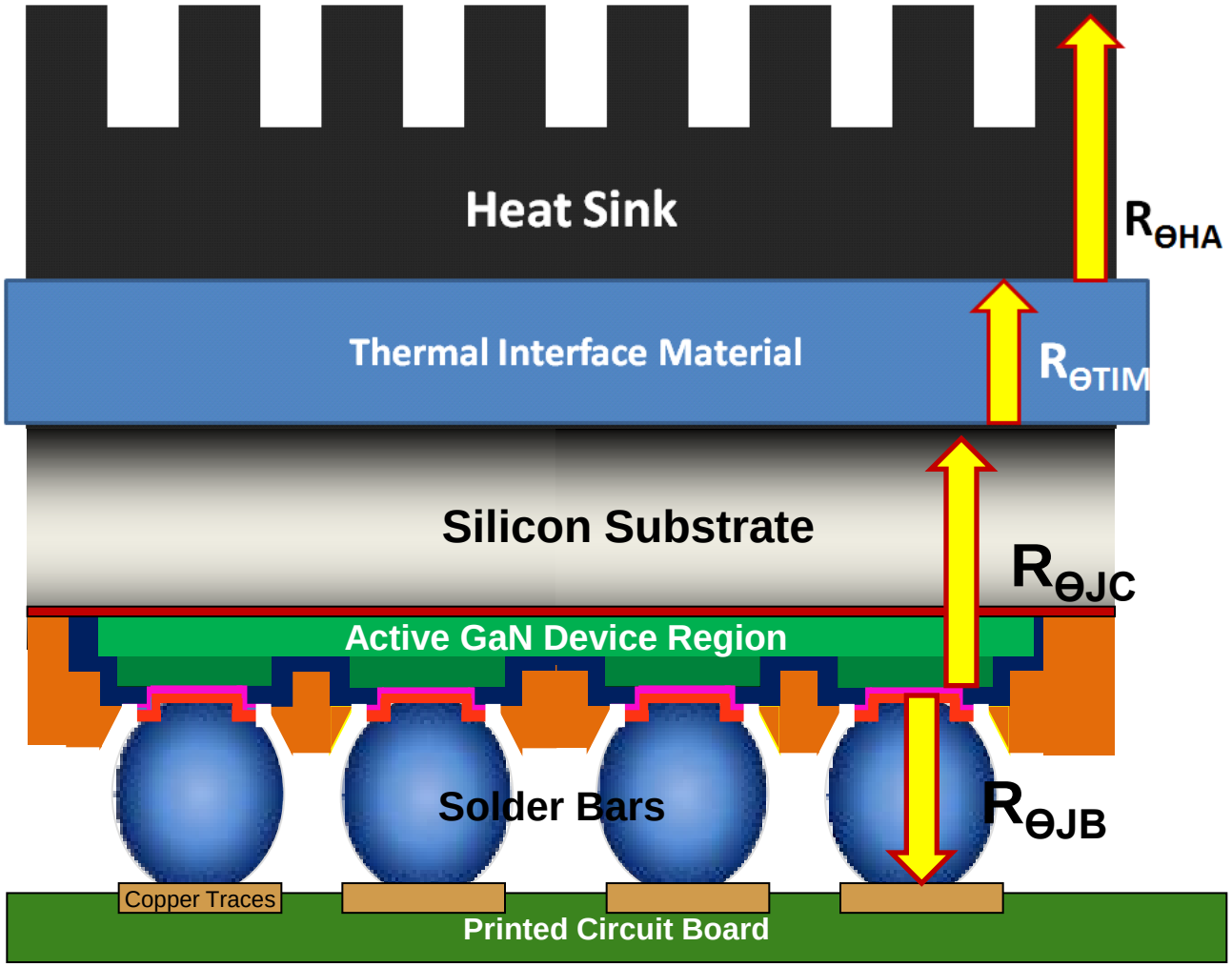


Thermal Management

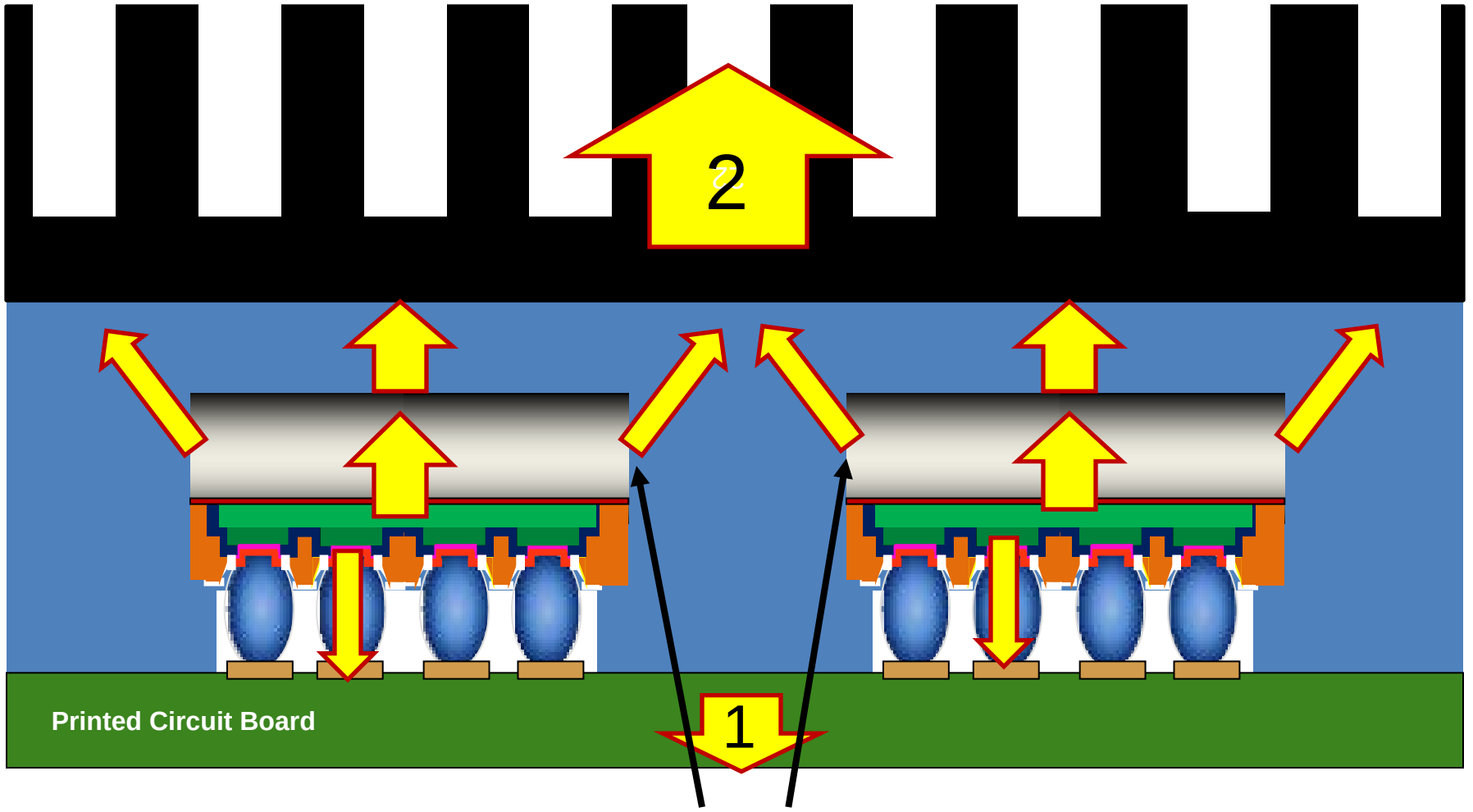


Two Paths For Heat: Through The Back Of The Die Or Through The Solder Contacts Into The PCB

Thermal Resistance with Heat Sink

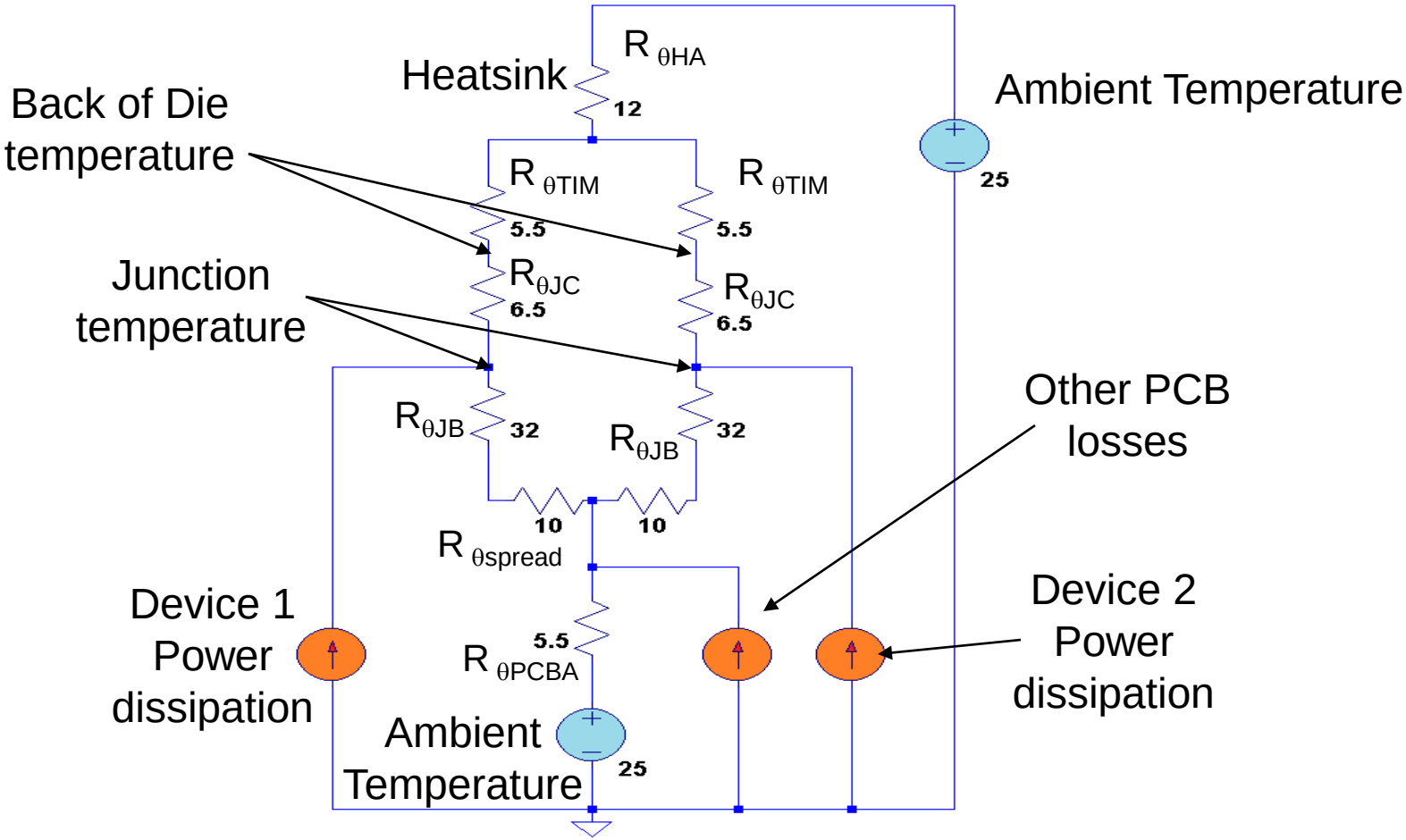


Thermal Resistance with Heat Sink

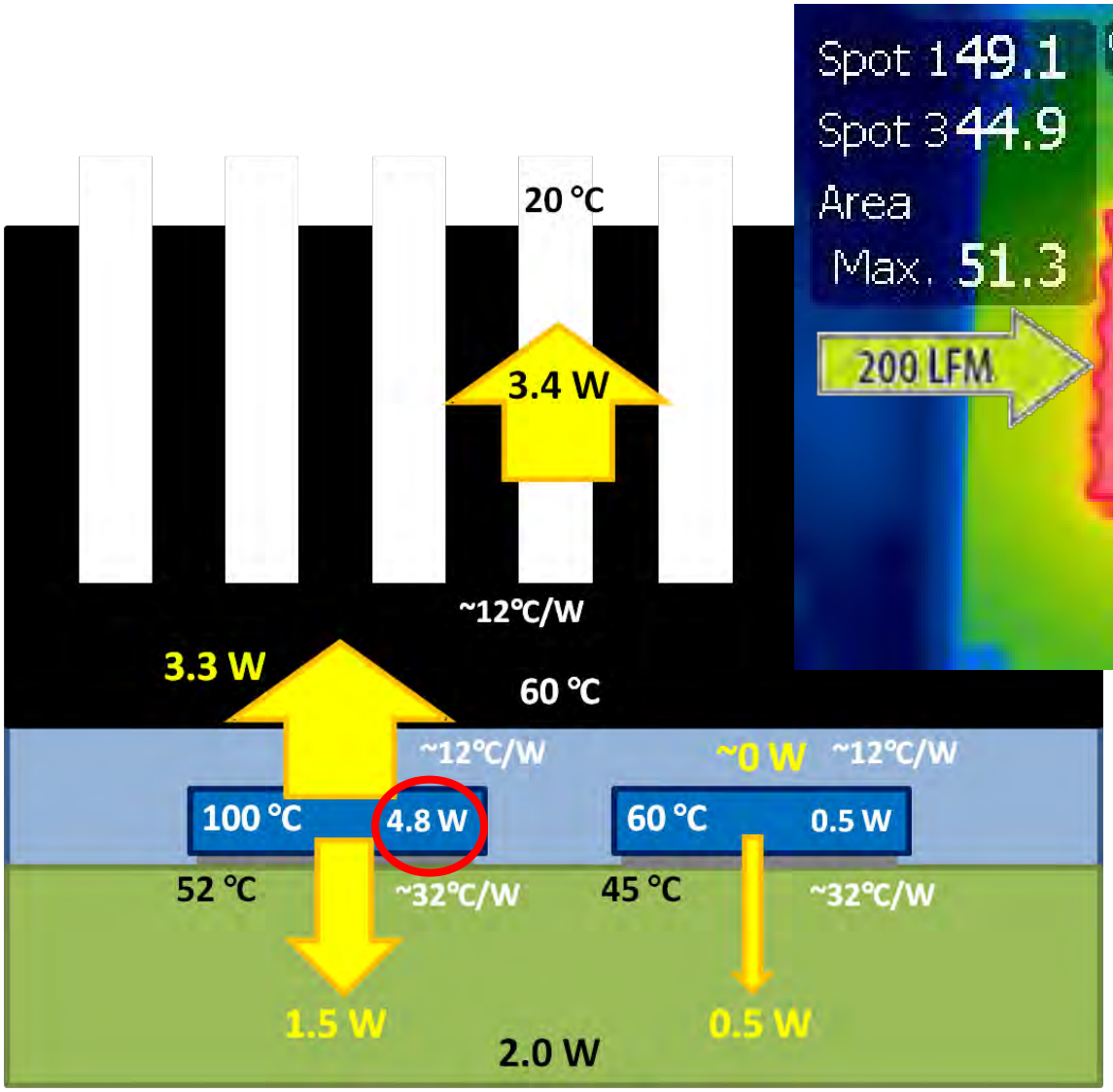


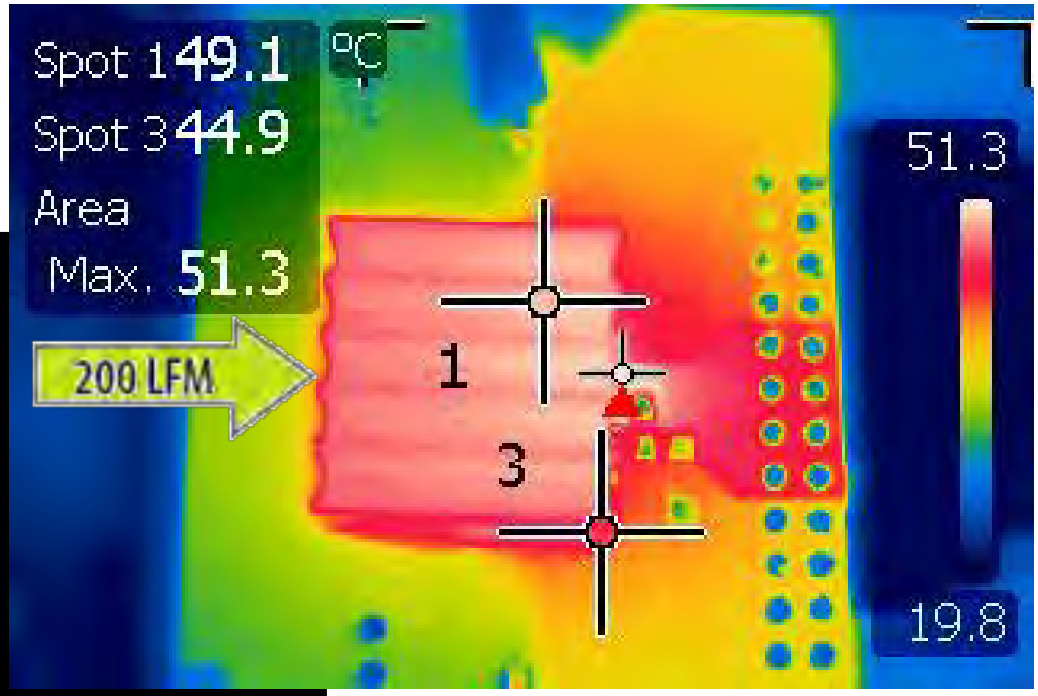
Thermal Interface Material on sides of die too

Thermal Model with Heat Sink



Thermal Results





Possible to remove up to 5 W from small EPC die with double sided cooling

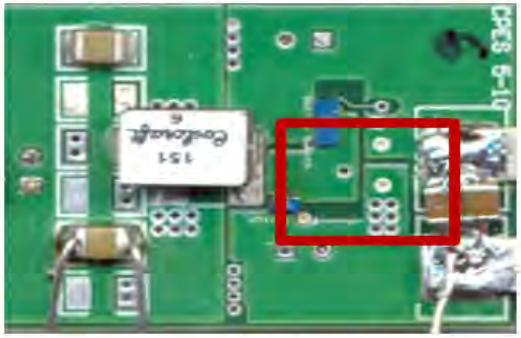
Design Example Agenda

- Hard Switched Circuits
  - Buck Converter
  - Isolated Full Bridge
  - Envelope Tracking
- Resonant Circuits
  - Intermediate Bus Converter

Buck Converters

High Frequency Buck Converters

CPES Gen 1

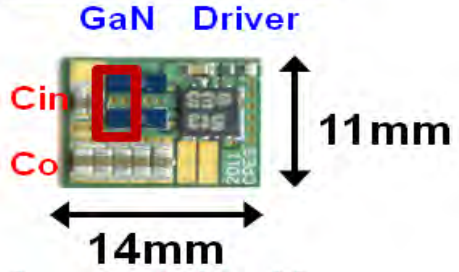


L_{Loop}=6.30nH

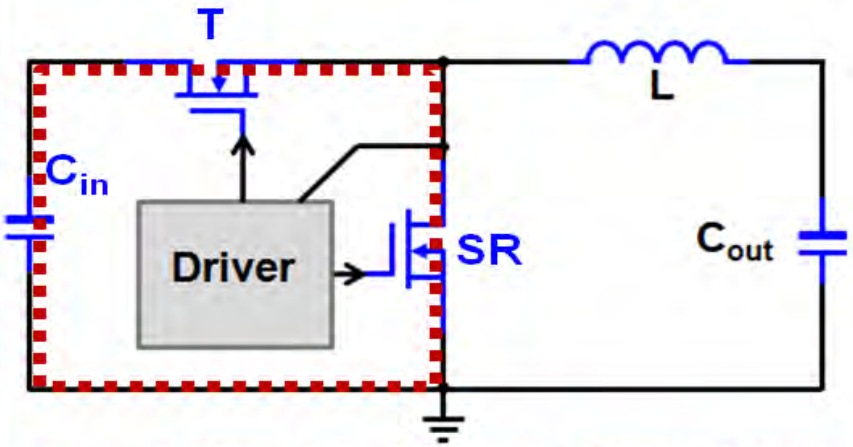
CPES Gen 2

L_{Loop}=2.90nH

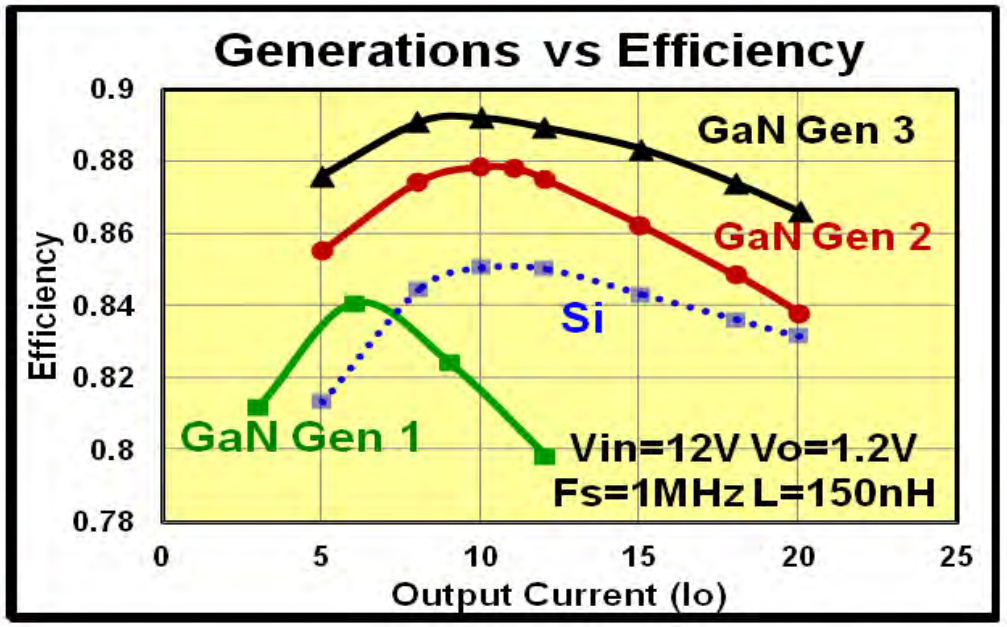
CPES Gen 3



L_{Loop}=1.19nH

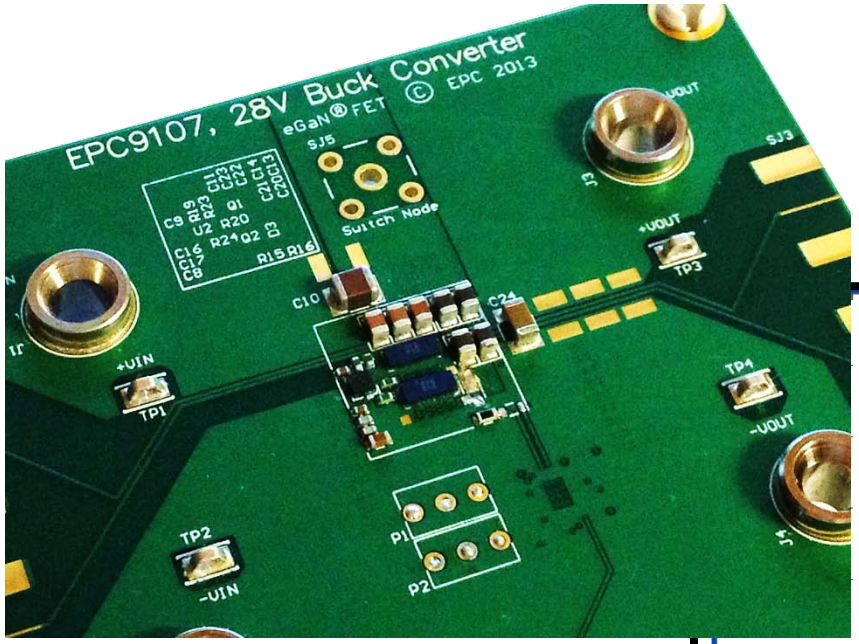


L_{Loop}: High Frequency Power Loop

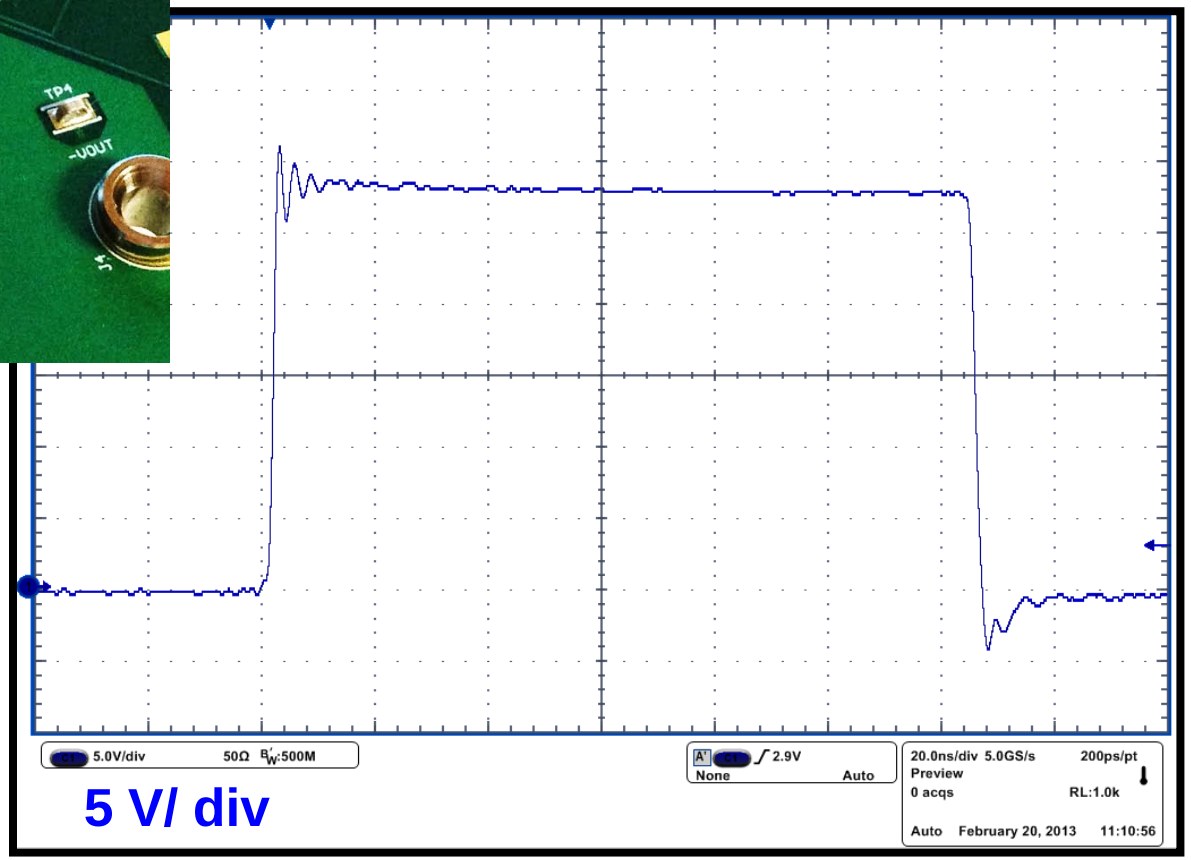


D. Reusch, D. Gilham, Y. Su, and F.C. Lee, C, "Gallium Nitride Based 3D Integrated Non-Isolated Point of Load Module", APEC 2012

EPC9107 Optimal Layout



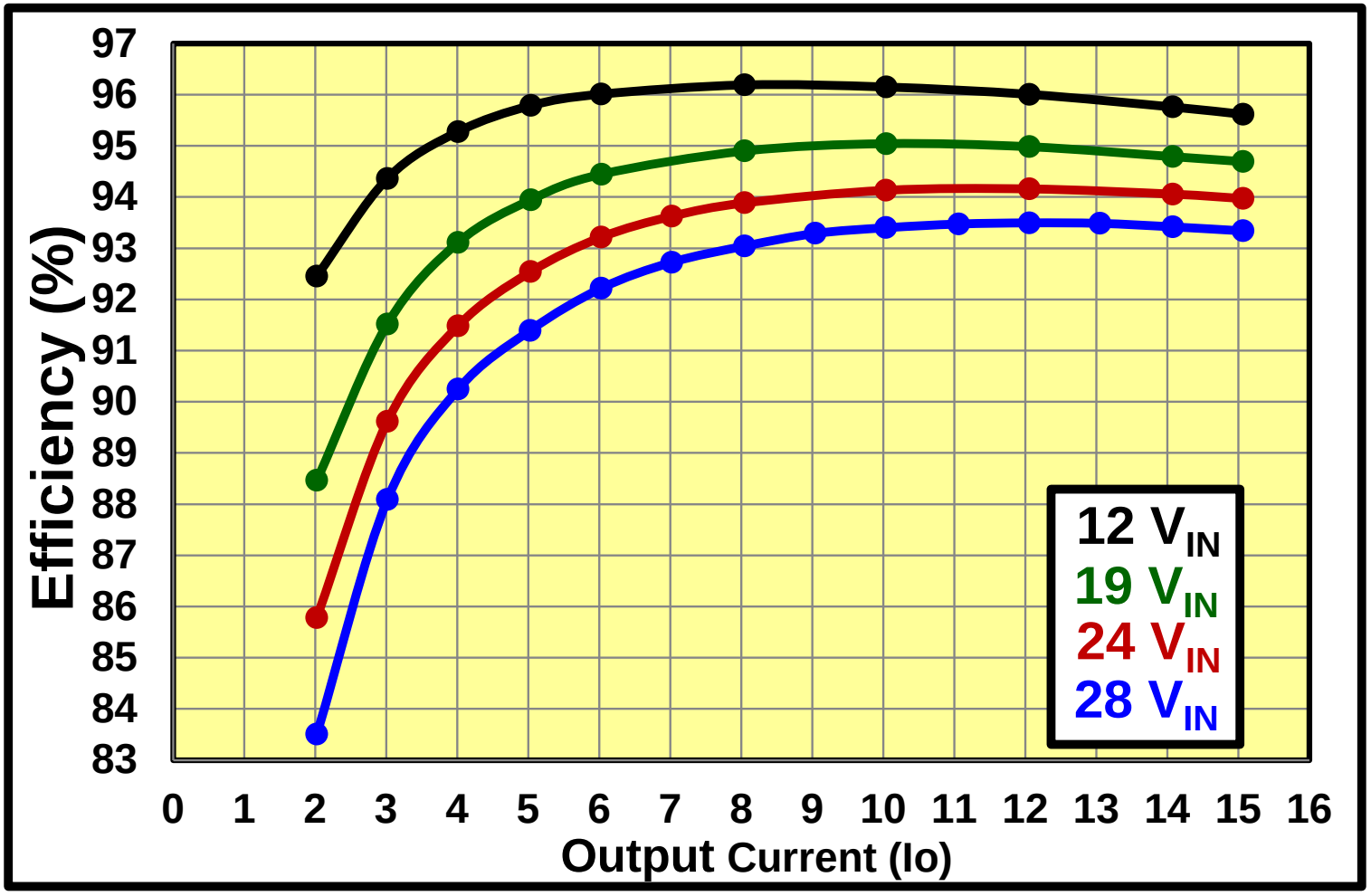
Buck Module
Switching Node Voltage
V_{IN}=28 V I_{OUT}=15 A



5 V/ div

EPC9107
Demonstration Board
V_{IN}=12-28 V V_{OUT}=3.3 V
I_{OUT}=15 A F_S=1 MHz
2 x EPC2015

EPC9107 Demonstration Board

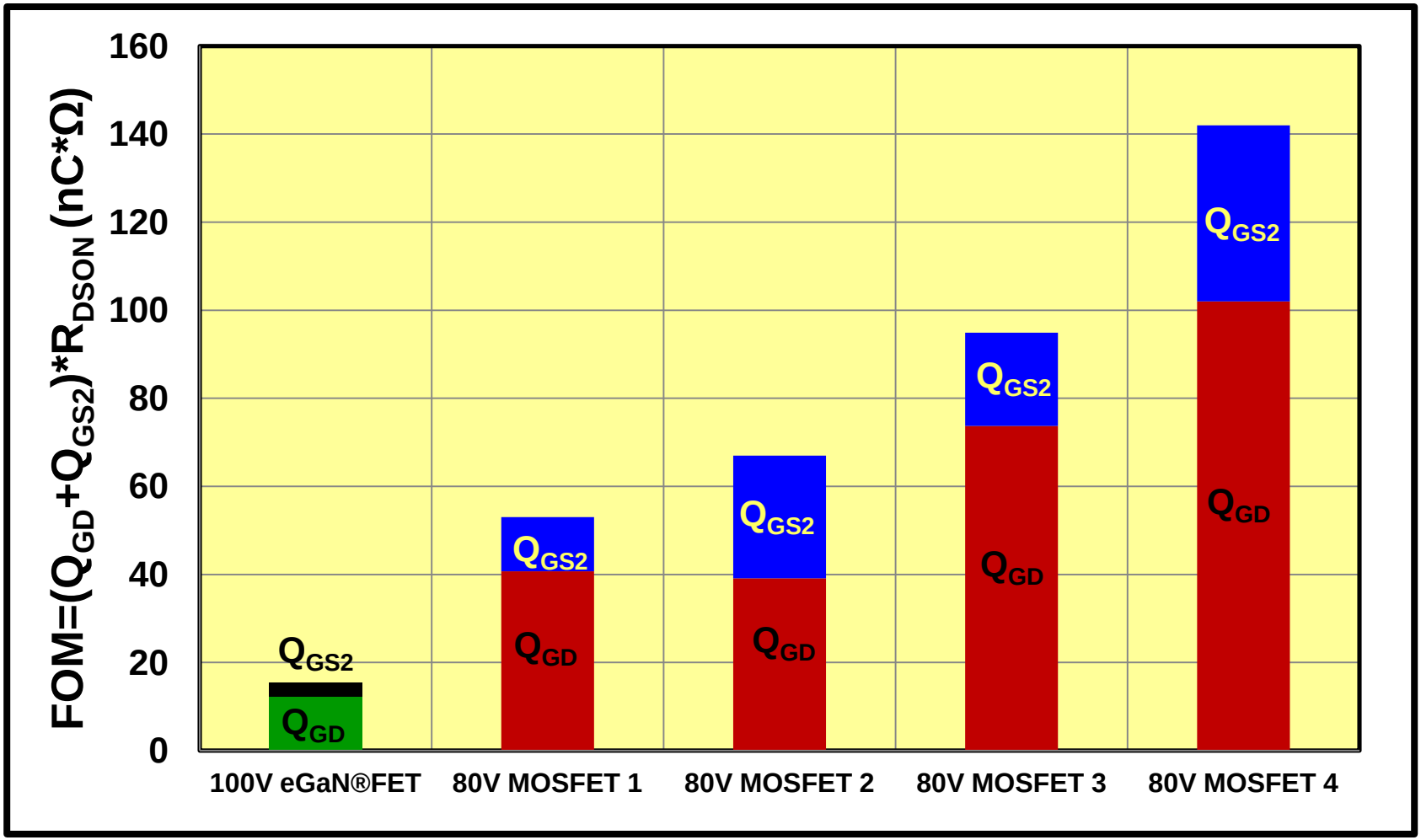


V_{OUT}=3.3 V F_S=1 MHz

GaN T/SR: EPC2015 Driver LM5113

Isolated Full Bridge

100 V Hard Switching FOM

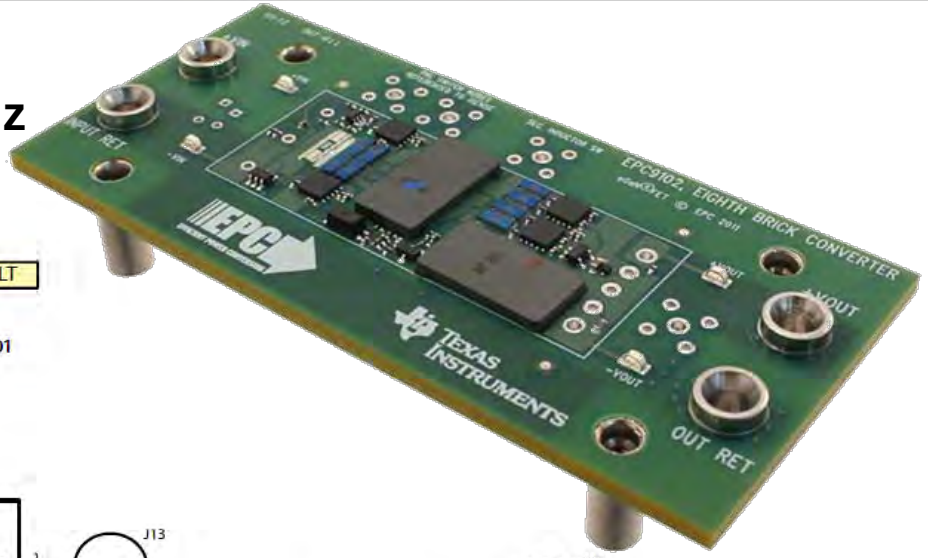


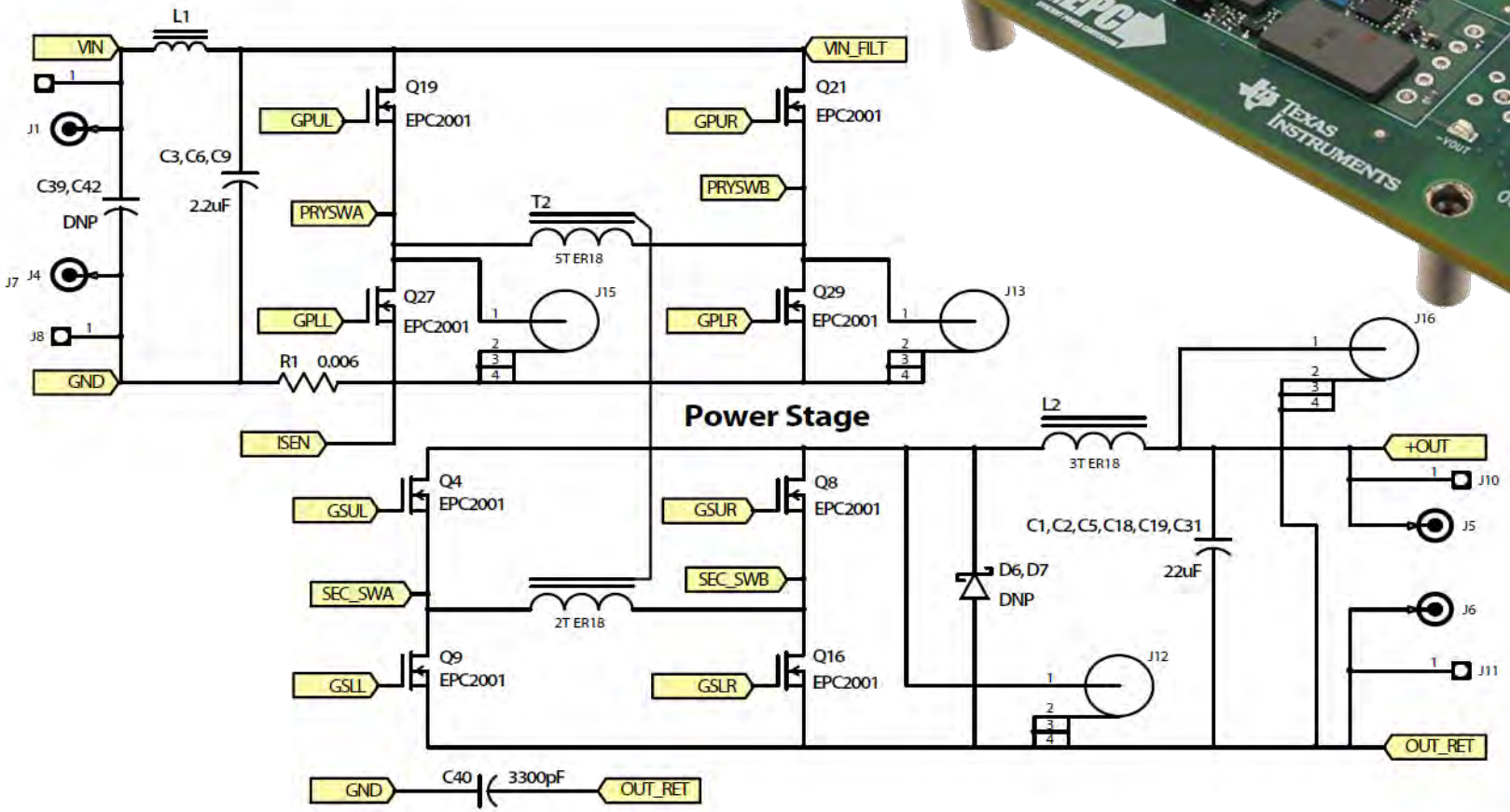
V_{DS}=0.5*V_{DS} , I_{DS}= 15 A

Regulated Full Bridge Converter

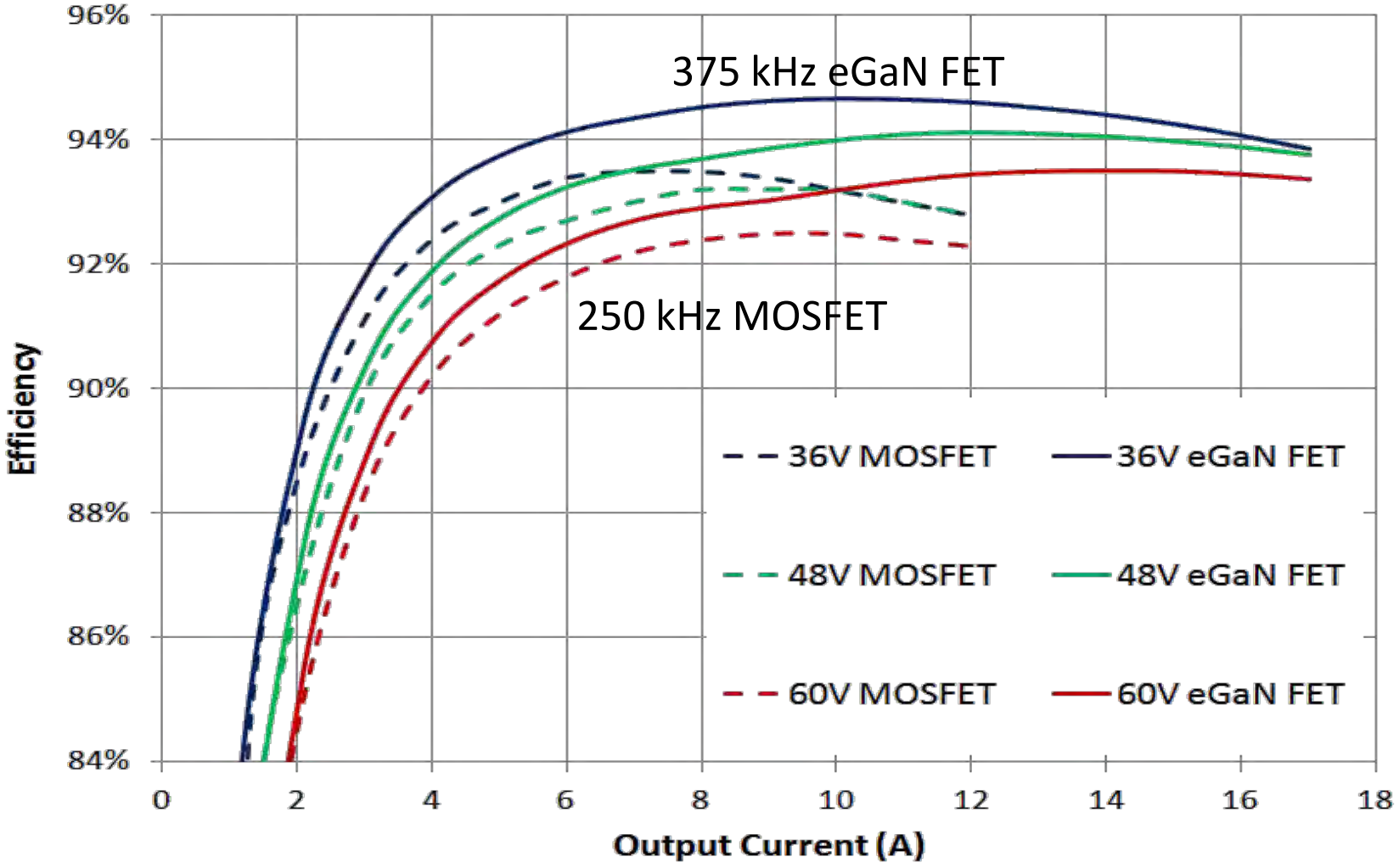
EPC9102 Demo board

Full Bridge, 36 - 60 Vin, 12 V, 200 W, 375 kHz





Efficiency Comparison



Regulated 12 V Output

Brick Converter Summary

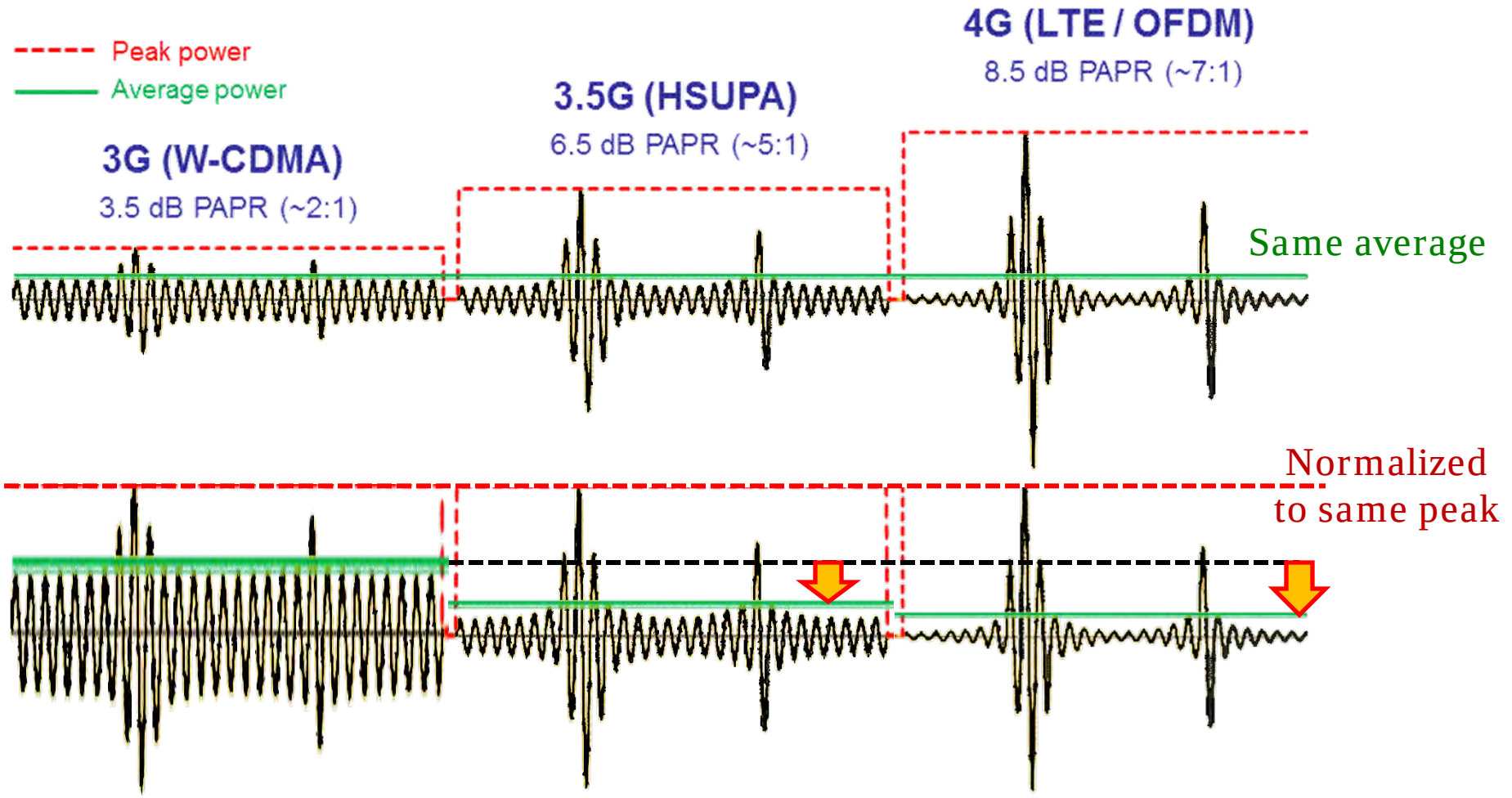
- Topologies varied
- Optimization as important as device selection
- Efficiency is key to power density
  - Maximum power loss is fixed.
- Good comparison requires identical designs
- Given topology, eGaN FETs will outperform MOSFETs based on superior FOM

Overview of Envelope Tracking

- World of Radio Frequency Power Amplifiers (RFPA) is changing.

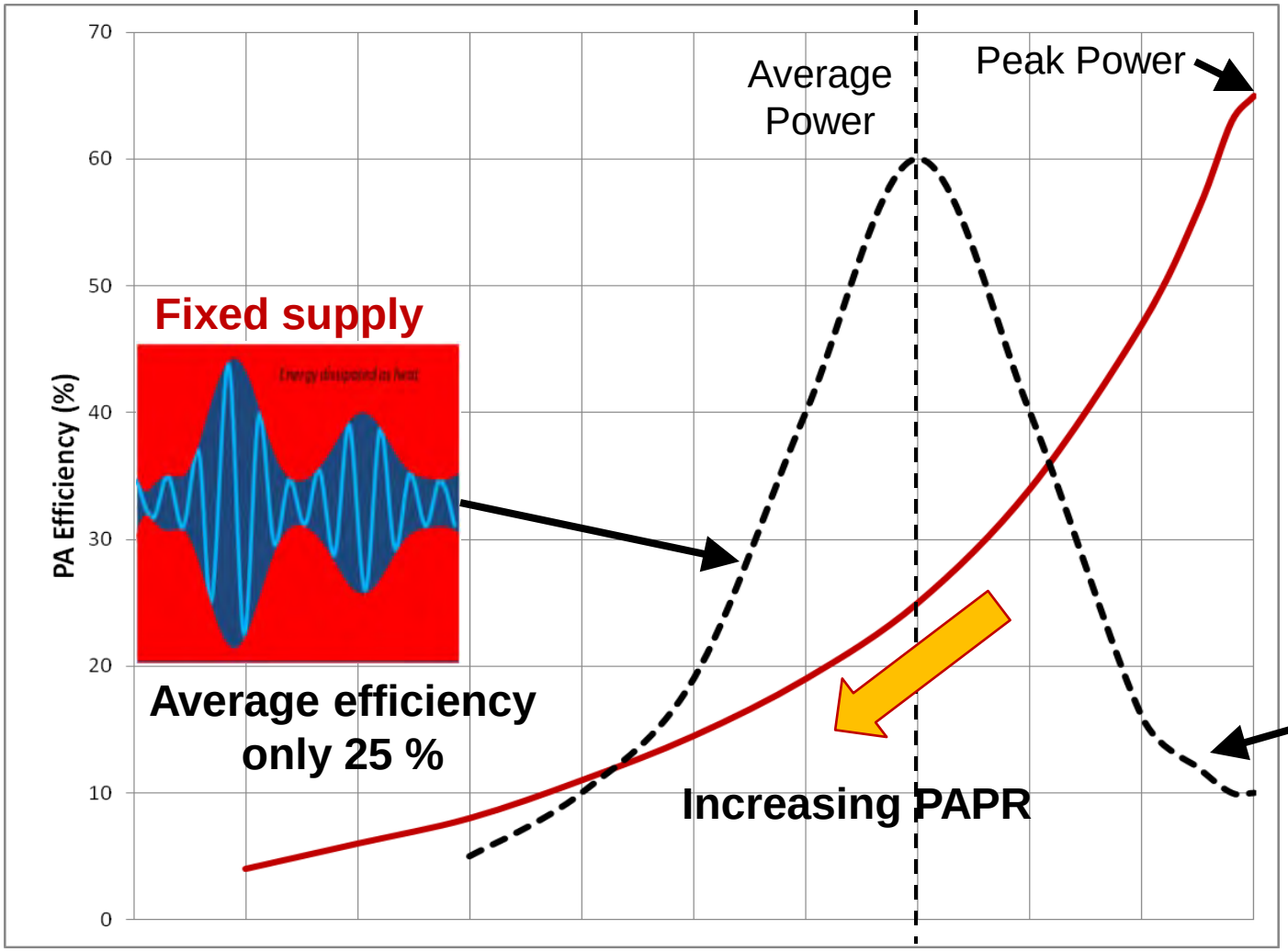
- Increased efficiency driven by:
  - Improved battery life
  - Reduced cooling
  - Reduced size
  - Lower cost of operation

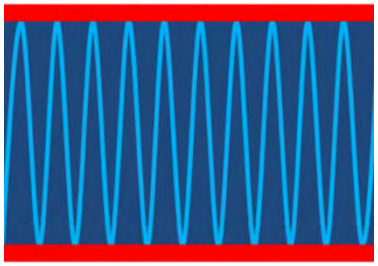
Peak to Average Power Ratio



Ref: Nujira.com website

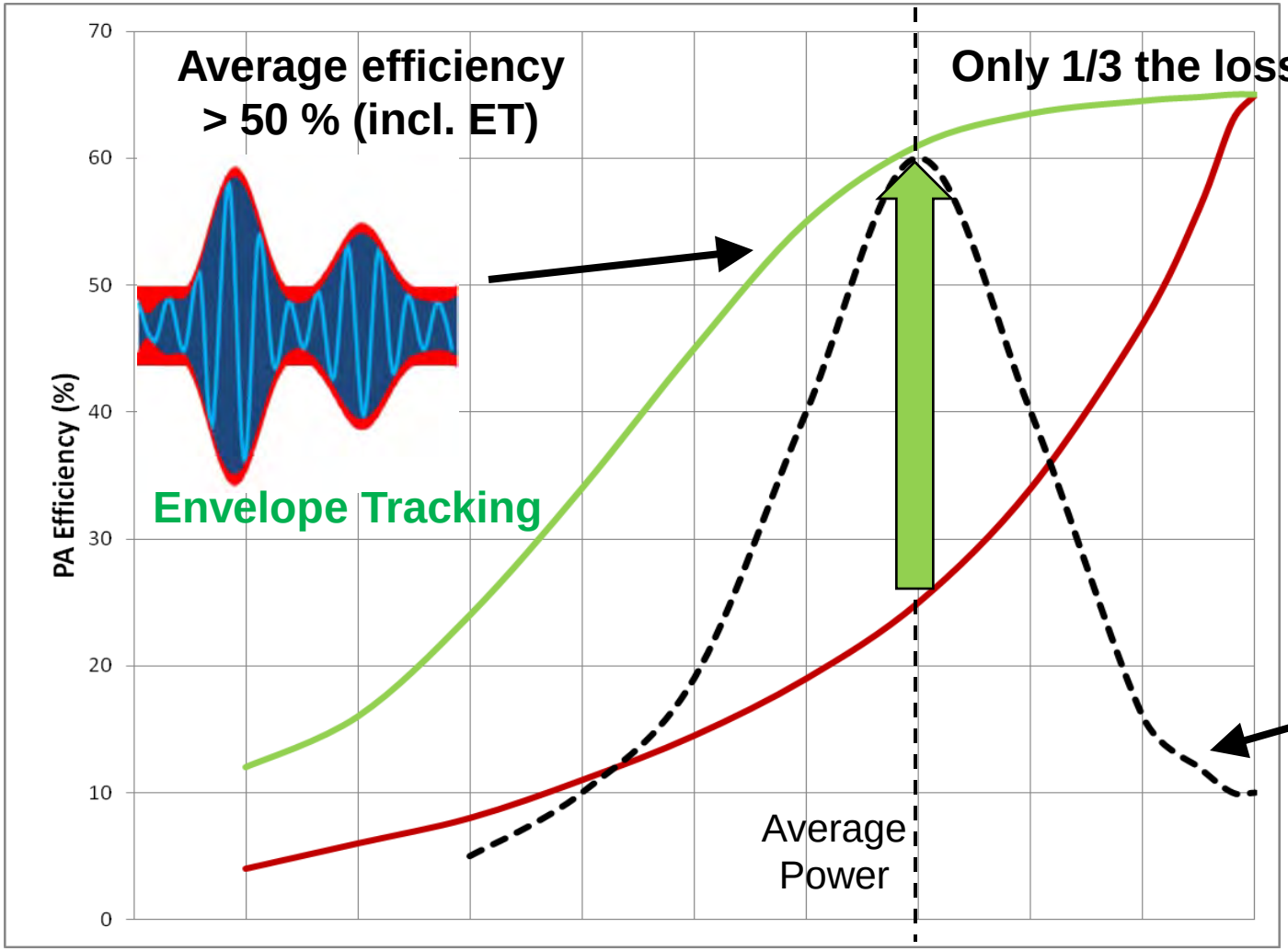
Effect of PAPR





PAPR = 0dB
Peak efficiency up to 65%

Effect of Envelope Tracking



RFPA Standards*

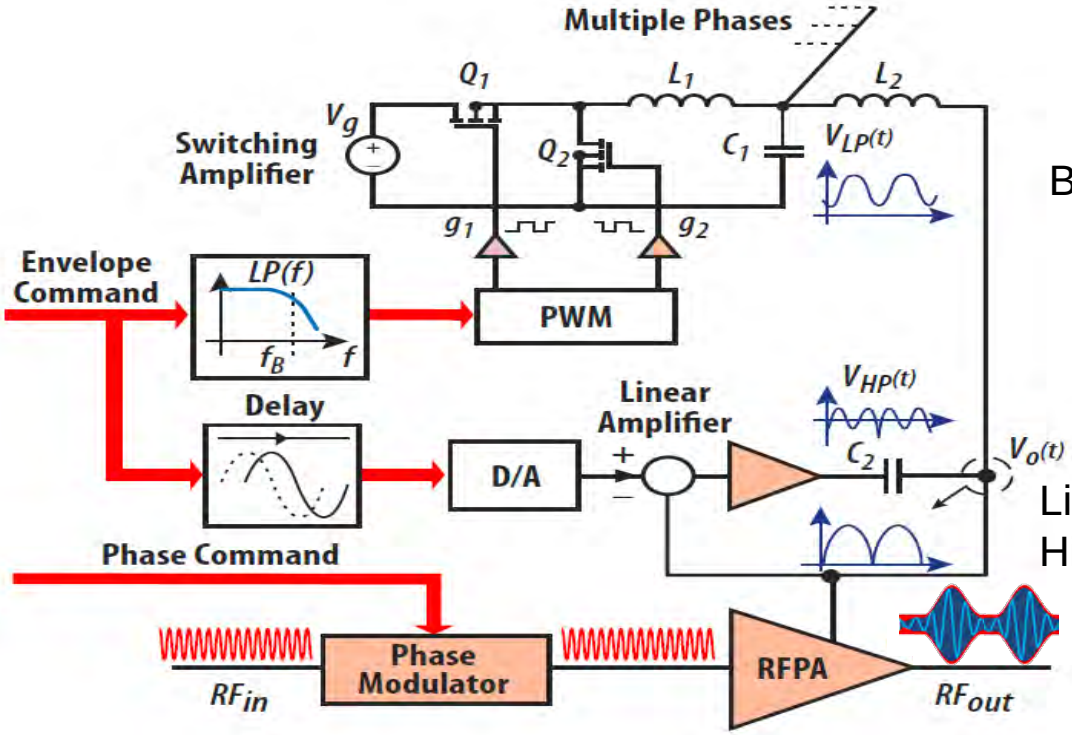
	Standard	Launched	Typ. Carrier BW (MHz)	Typ. Spectral Efficiency (bps/Hz)	Approx. PAPR(dB)
2G cellular	GSM	1991	0.2	0.17	0.0
2.75G cellular	GSM + EDGE	2003	0.2	0.33	3.5
3G cellular	WCDMA FDD	2001	5	0.51	7.0
Digital TV	DVB-T	1997	8	0.55	8.0
Wi-Fi	IEEE 802.11a/g	2003	20	0.90	9.0
WiMAX	IEEE 802.16d	2004	20	1.20	8.5
Wi-Fi	IEEE 802.11n	2007	20	2.40	9.0
3.5G cellular	HSDPA	2007	5	2.88	8.0
3.9G cellular	LTE	2009	20	8.00	10.0

- Up to 20 MHz Carrier bandwidth required
- Required ET supply BW up to 5x higher if linear control

***Ref: www.open-et.org website**

Envelope Tracking Supply

- ET power supply topologies vary
  - Open loop boost – full BW required
  - Closed loop linear-assisted Buck*



Buck ~ 10% Bandwidth
~ 90% Power

Linear AMP ~ 10% Power
Highest 90% of Bandwidth

***V. Yousefzadeh, et. Al, Efficiency optimization in linear-assisted switching power converters for envelope tracking in RF power amplifiers, ISCAS 2005**

eGaN® FET based Buck(s) for ET

1300 W DVB* – 8 MHz BW and 8 dB PAPR

Linear-assisted Buck for ET

- 4 phase x 1 MHz Buck with up to 800 kHz band width
- 45 V_{IN}, 22 V_{OUT}/ 15 A_{OUT} (Avg)

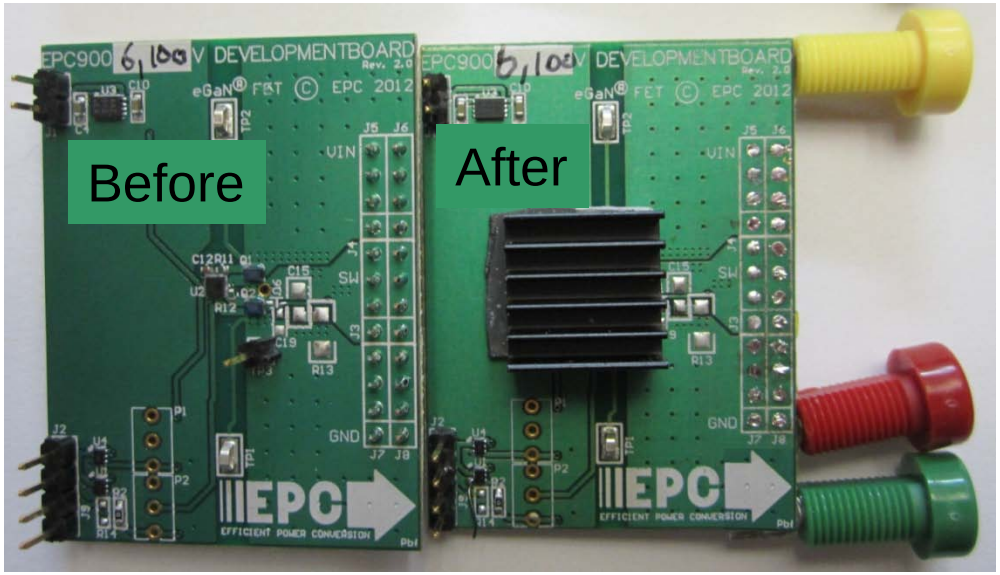
Pure Buck option for ET (Push frequency)

- 10 phase x 4 MHz Buck with up to 8 MHz band width
- 45 V_{IN}, 22 V_{OUT}/ 6 A_{OUT} (Avg)

***Representative of a high power ET buck in HV LDMOS, such as that implemented by ET specialist Nujira.**

6 A_{OUT} / 4 MHz Single ϕ Buck

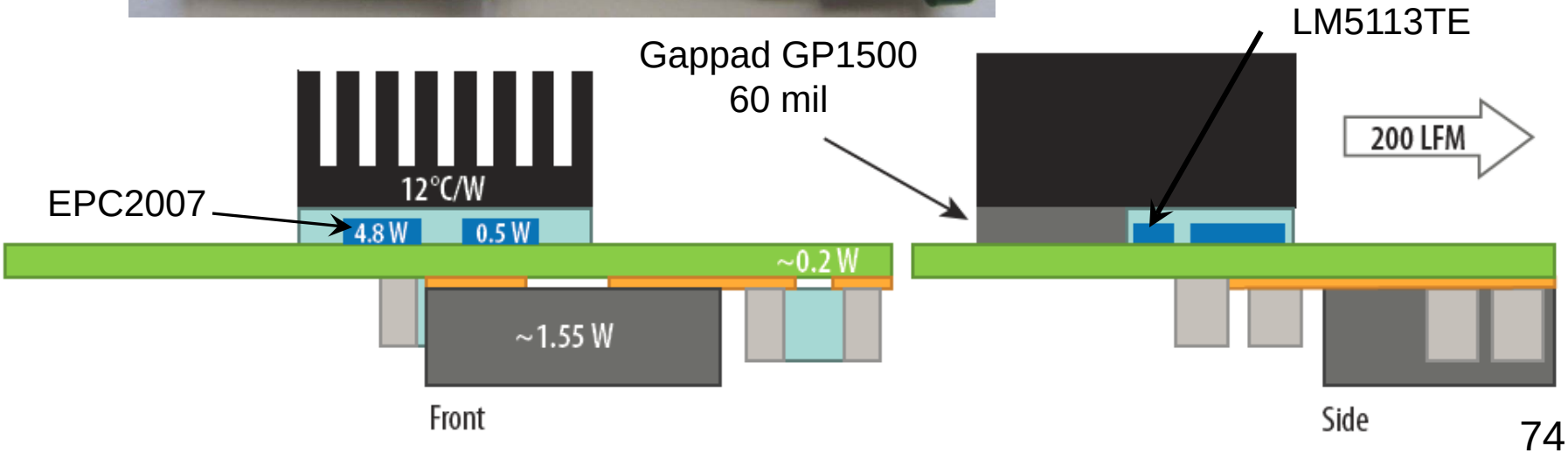
- Modified an EPC9006 development board



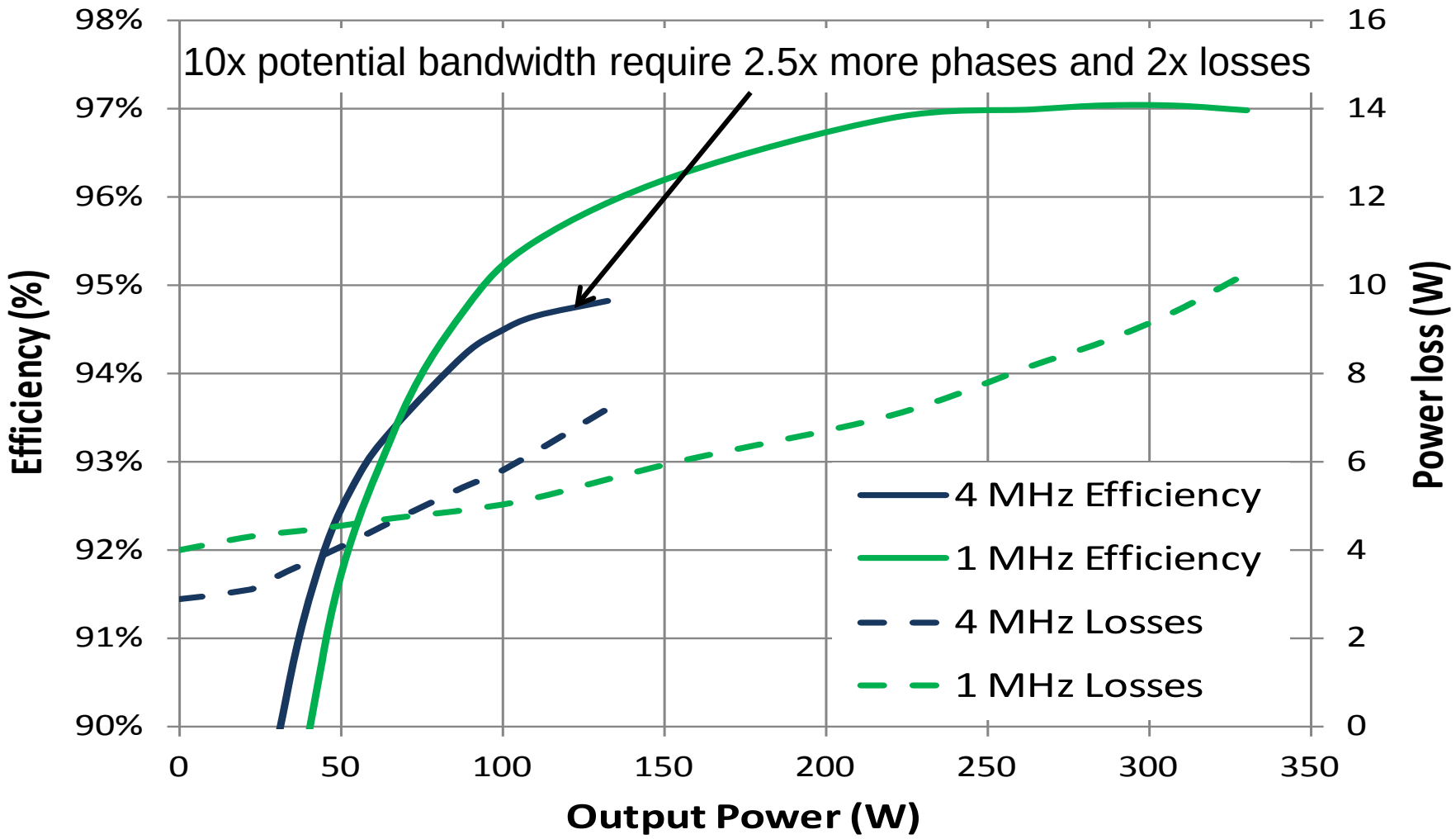
45 V_{IN}

22 V_{OUT}

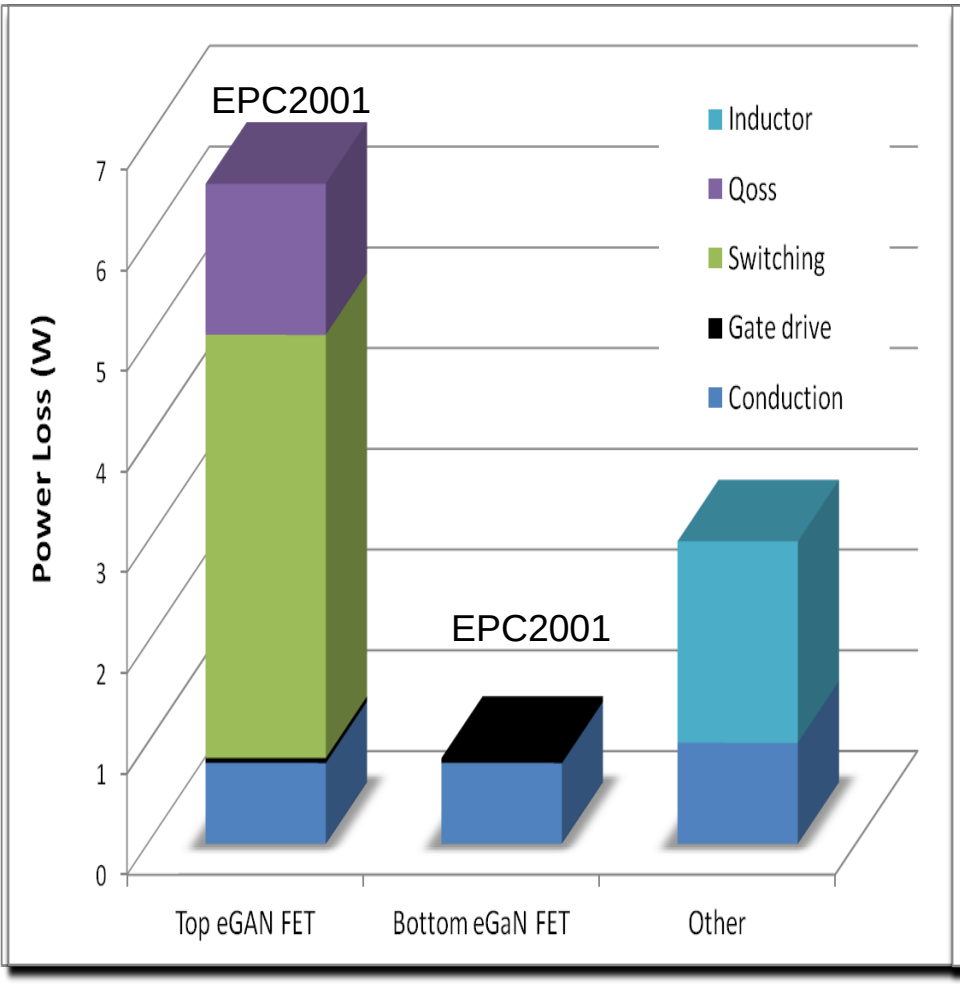
Common



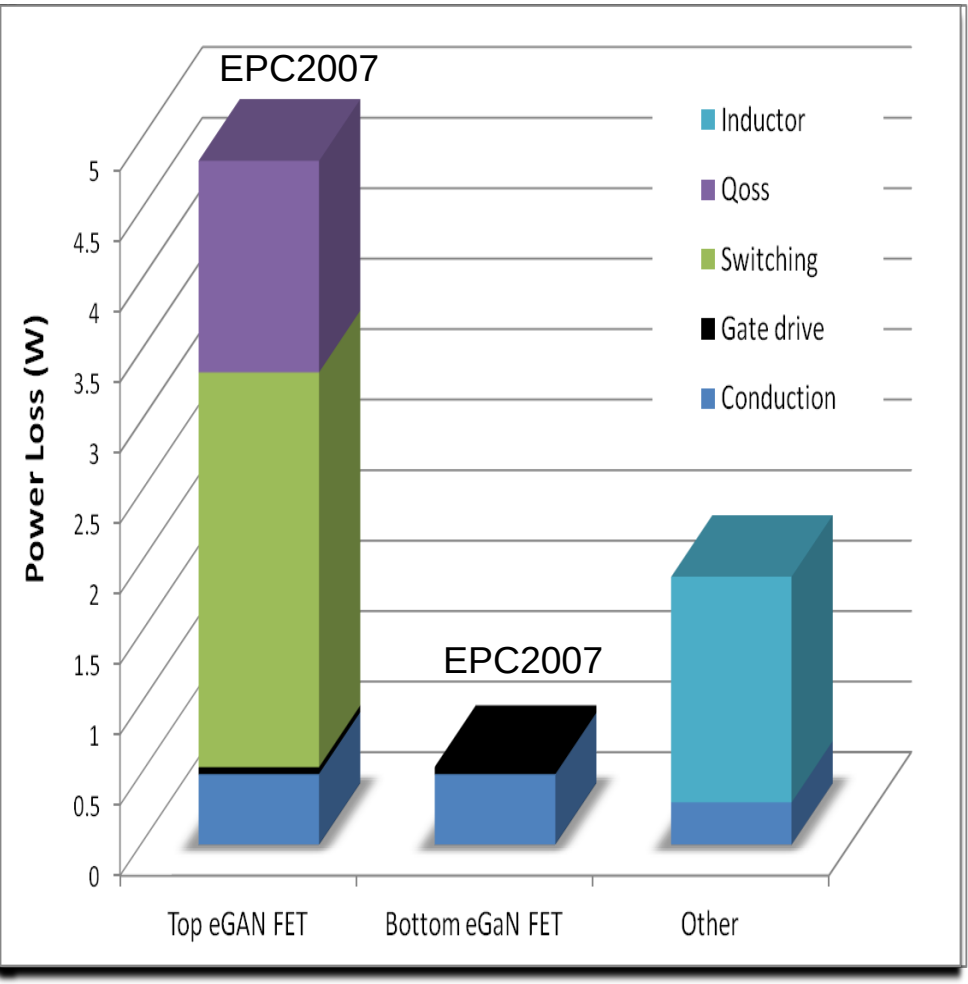
Efficiency Results



Loss Breakdown



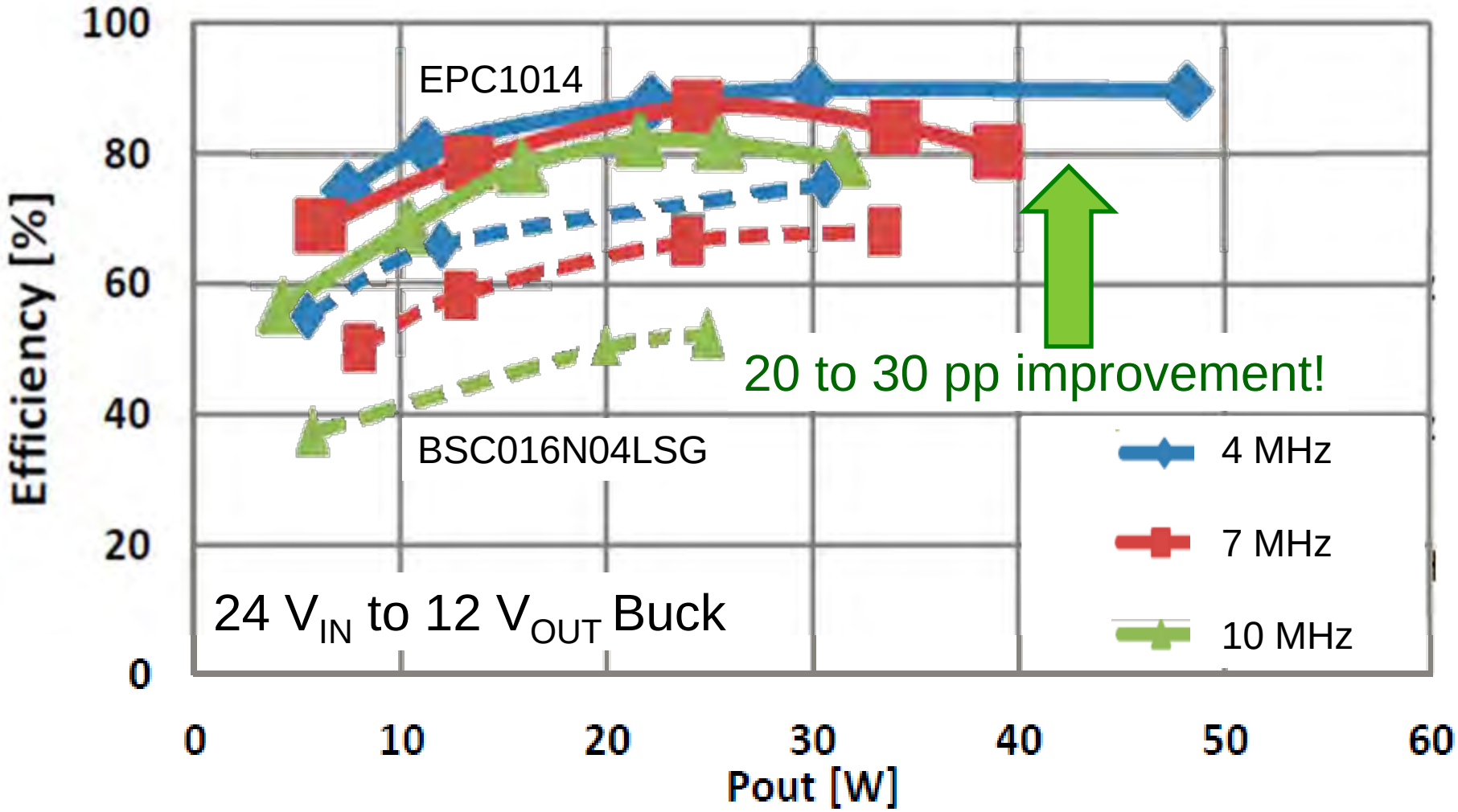
1 MHz EPC9002



4 MHz EPC9006

Future die size optimization possible

Higher Frequency ET Results*



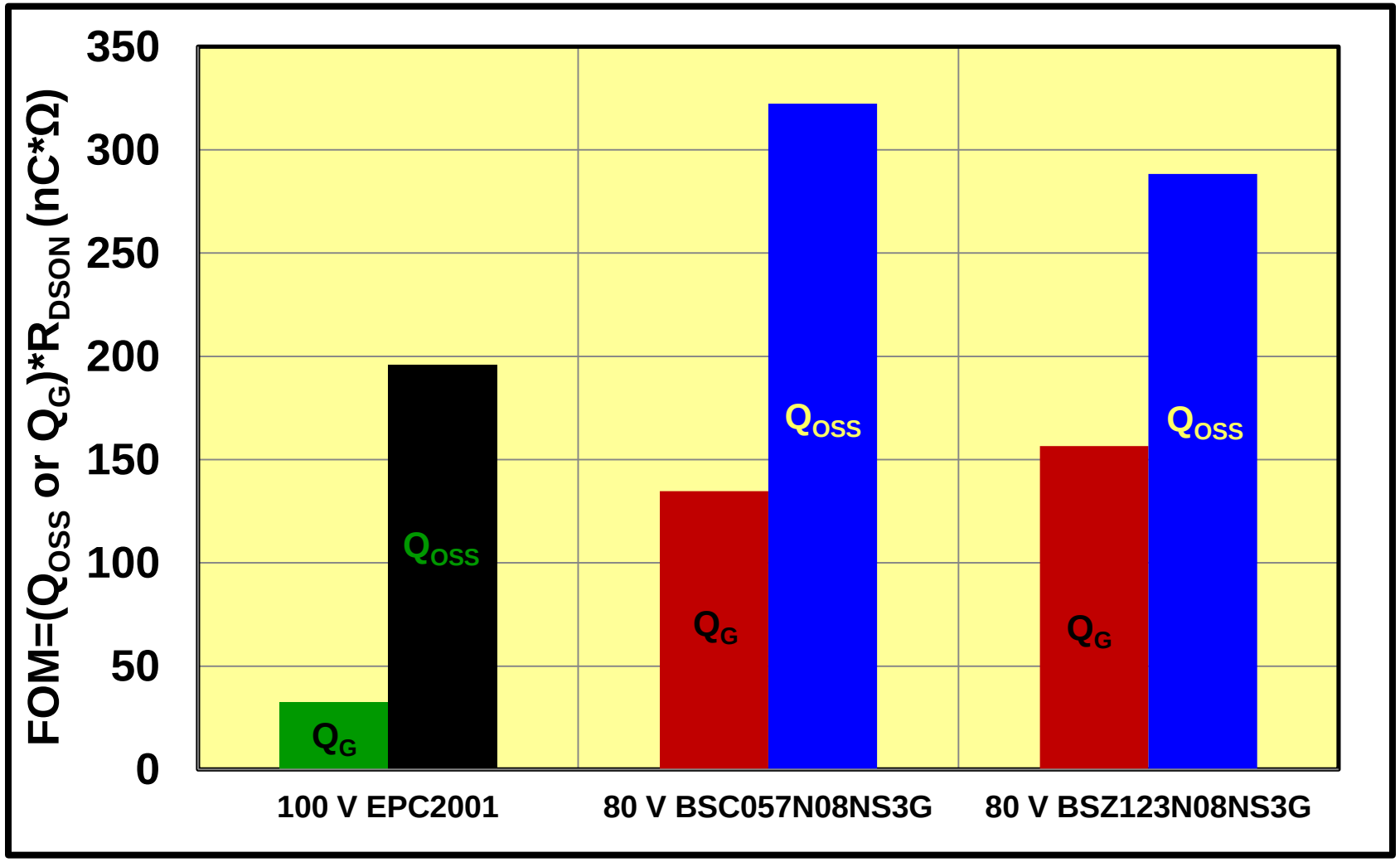
*D. Čučak, et. al, "Application of eGaN FETs for highly efficient Radio Frequency Power Amplifier", CIPS 2012

Envelope Tracking Summary

- eGaN FETs are an enabling technology for ET
  - Low charge reduces delay and switching times
  - Thermally possible - with double sided cooling
- Results are representative, but not optimized
  - Improve inductor selection
  - Improve thermal design
  - Reduce high side peak device temp by reducing low side device size to reduce Q_{OSS} losses
- Power and # of phases application specific

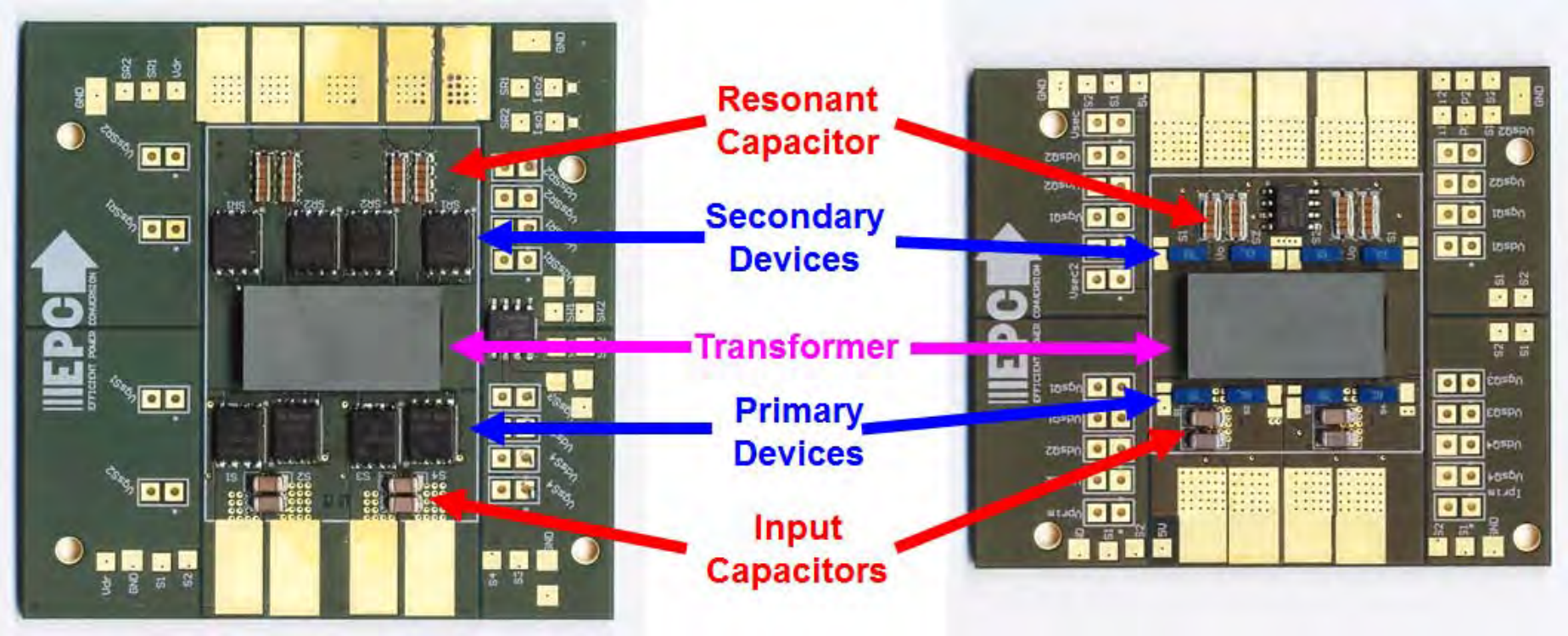
Resonant Converters

100 V Soft Switching FOM

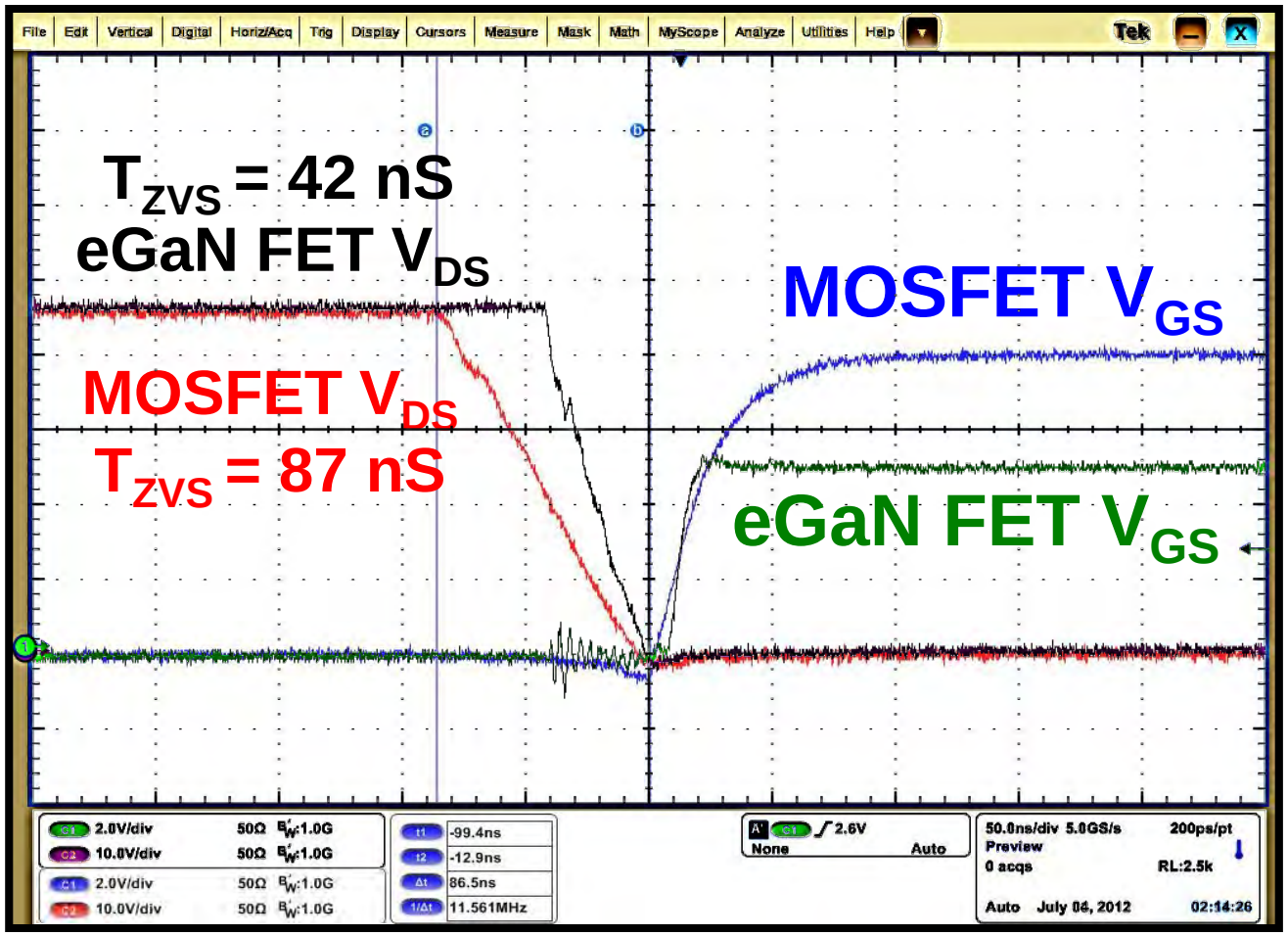


V_{DS}=48 V

eGaN® FET vs. MOSFET

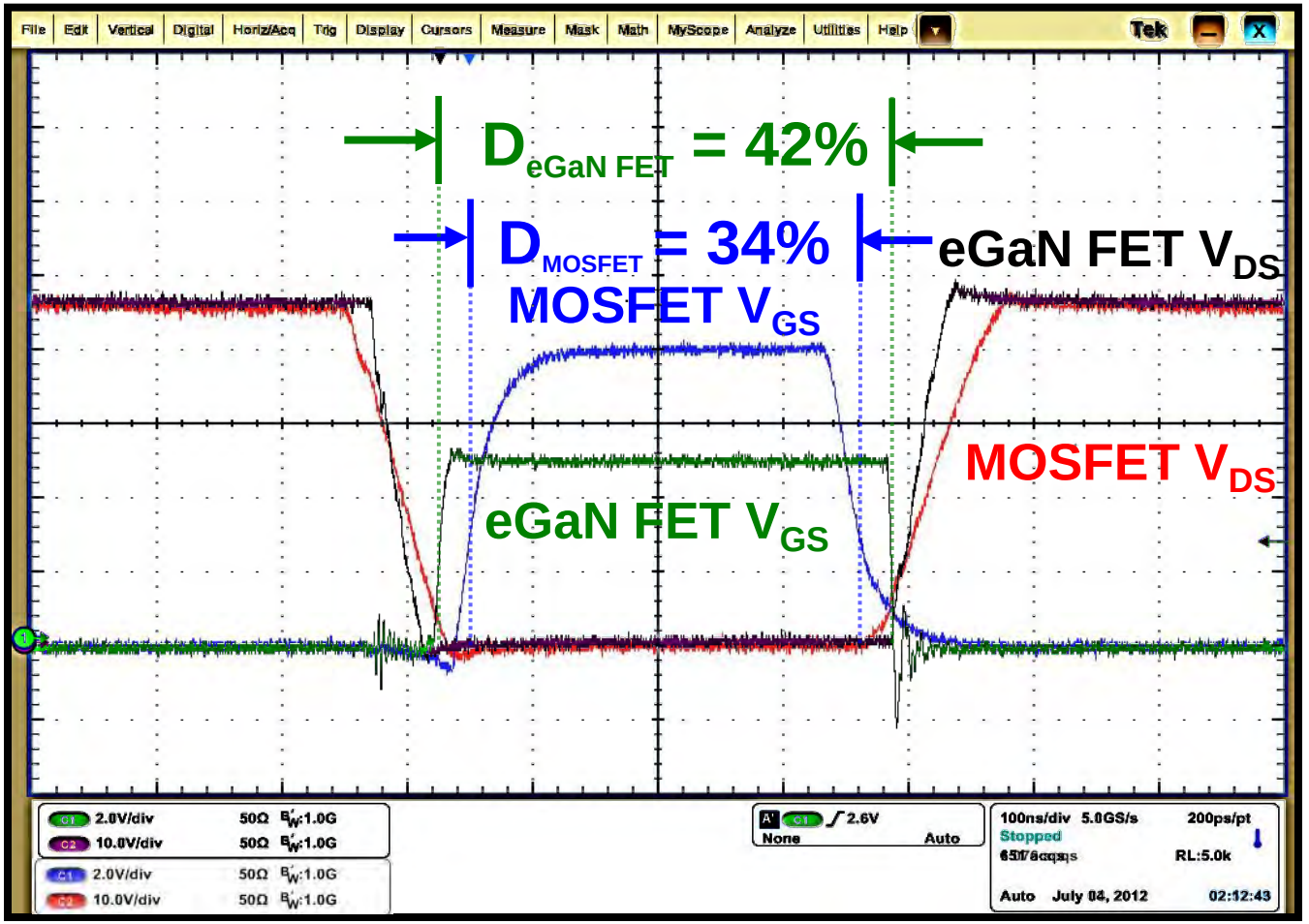


ZVS Switching Comparison



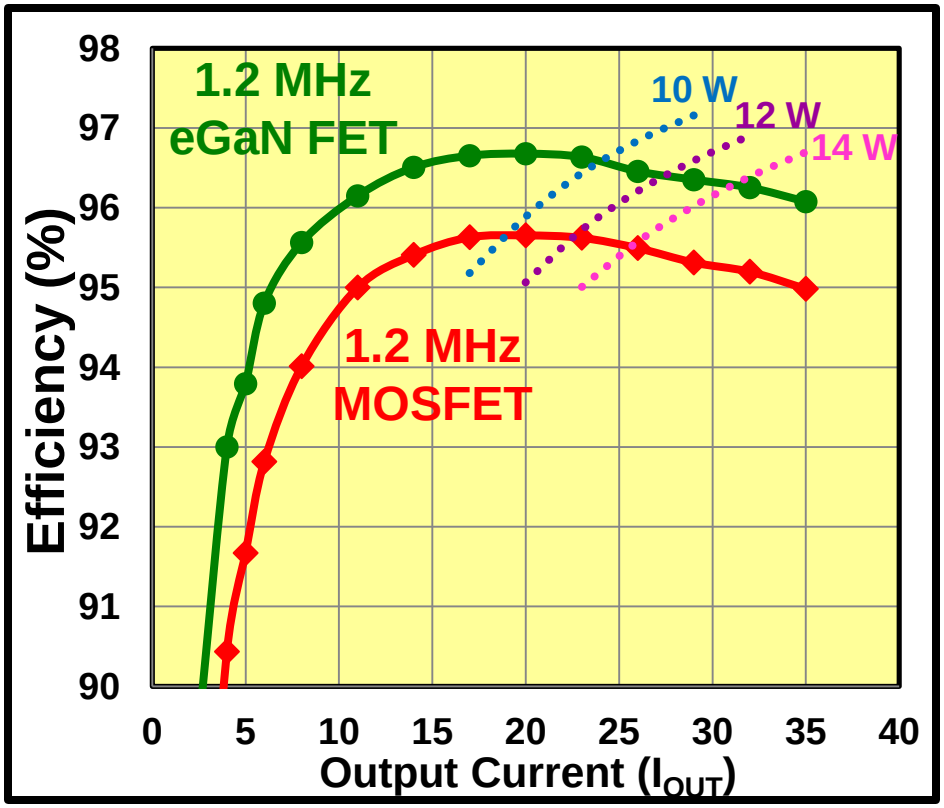
F_S = 1.2 MHz, V_{IN} = 48 V, and V_{OUT} = 12 V

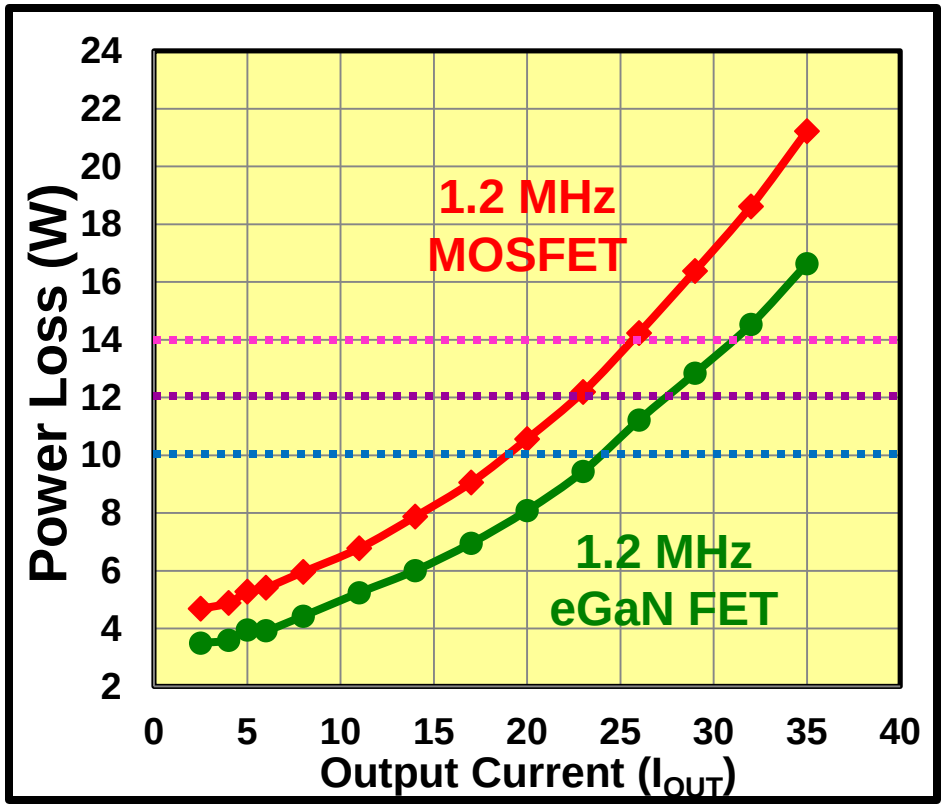
Duty Cycle Comparison



F_S = 1.2 MHz, V_{IN} = 48 V, and V_{OUT} = 12 V

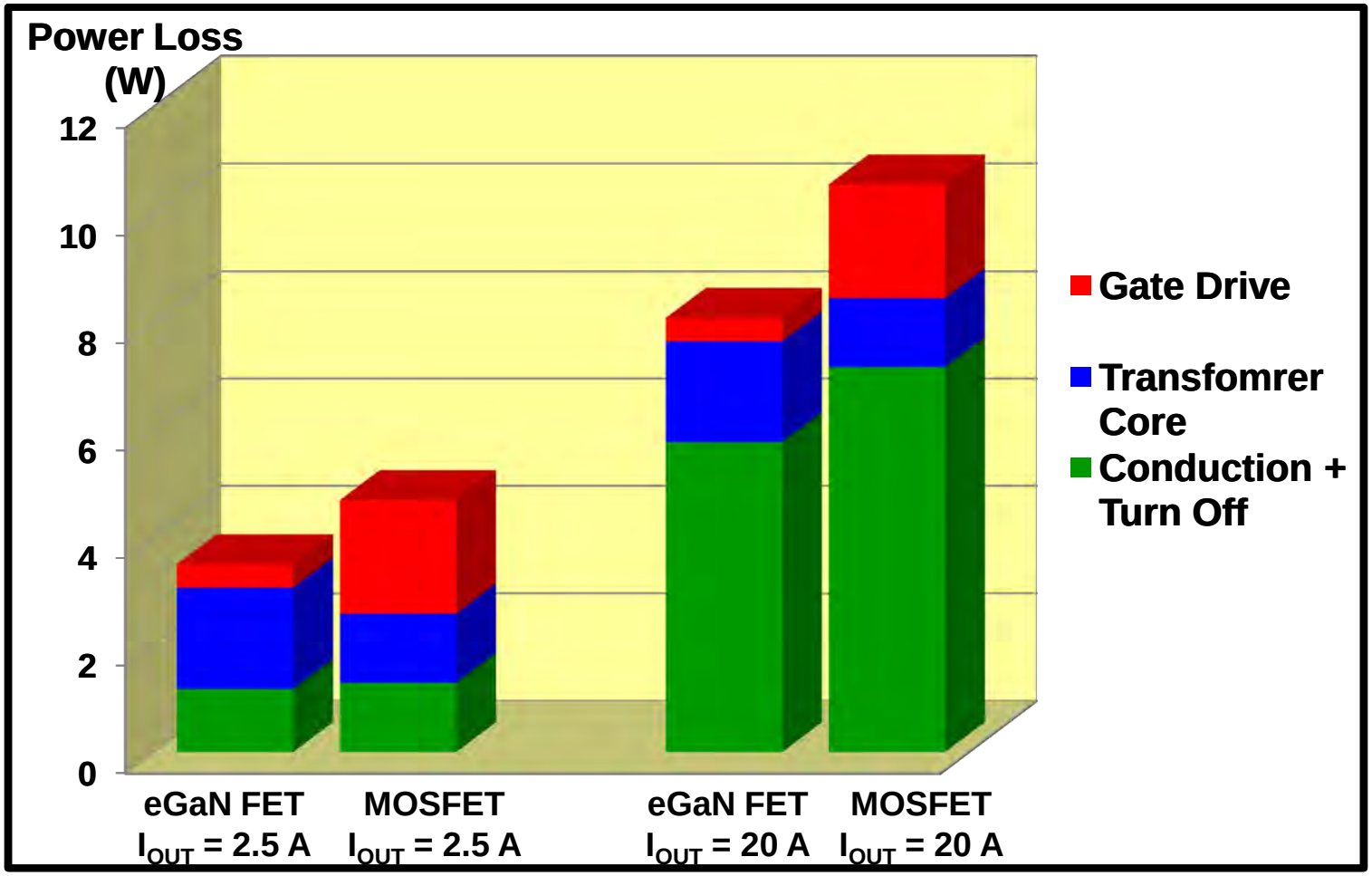
Efficiency Comparison





F_S = 1.2 MHz, V_{IN} = 48 V, and V_{OUT} = 12 V

Loss Breakdown

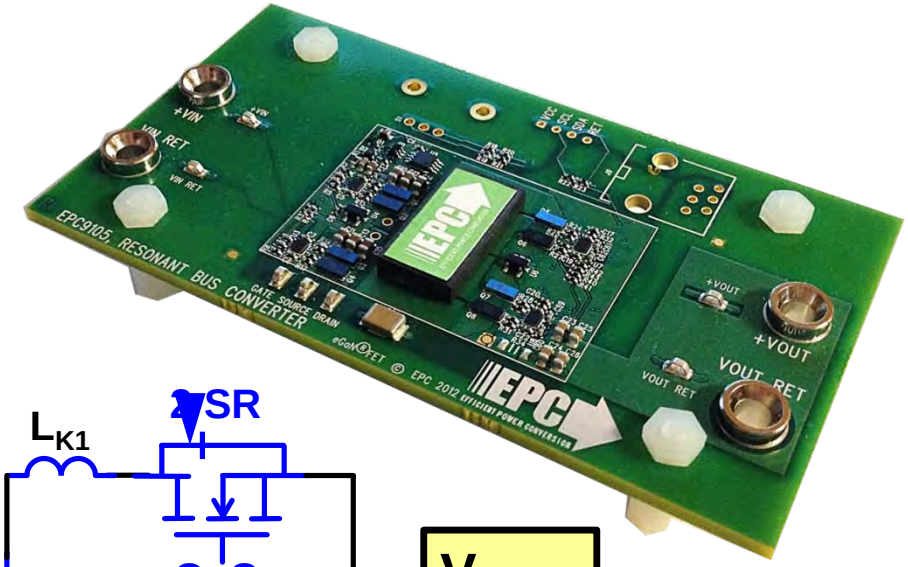


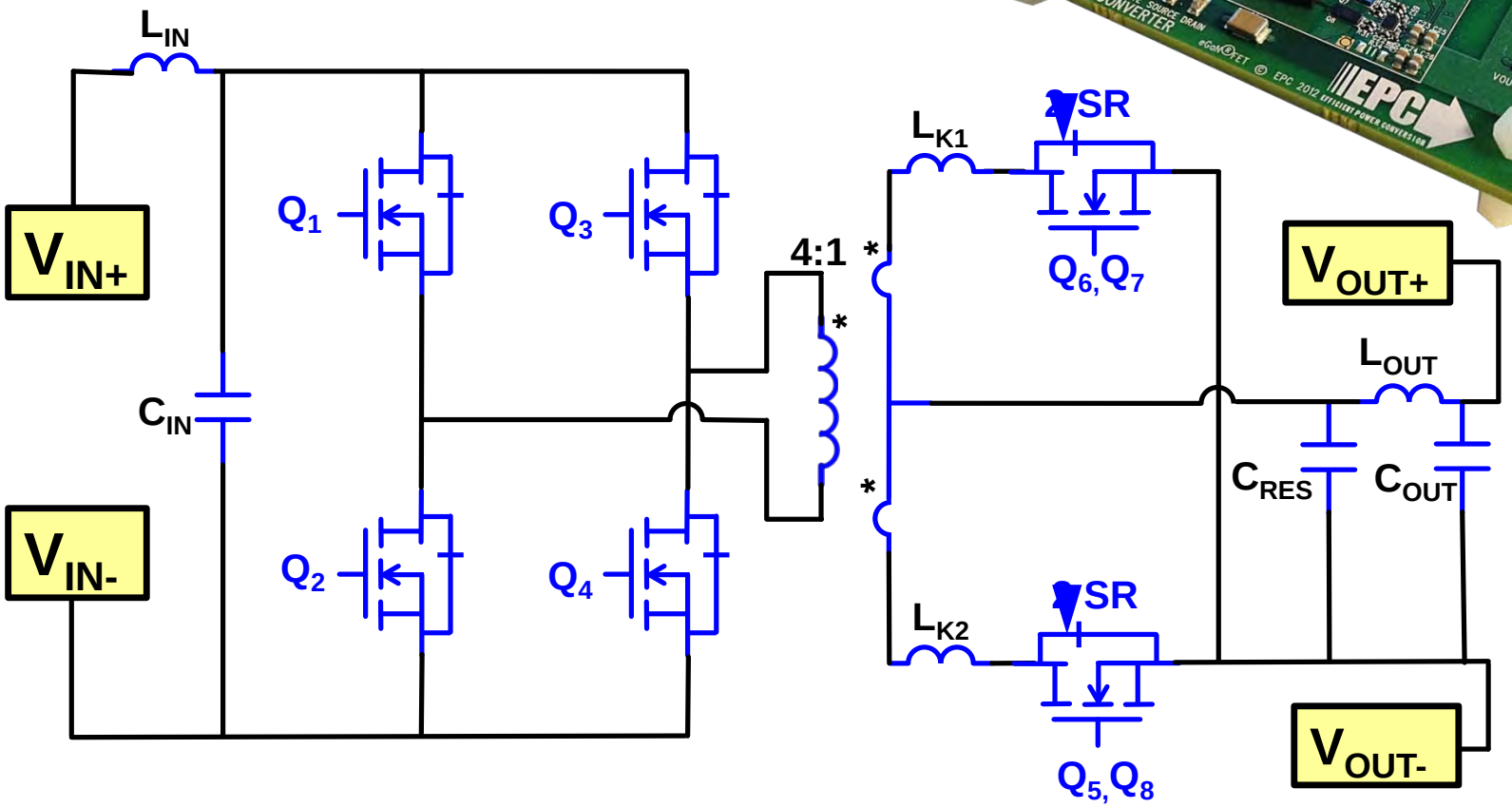
F_S = 1.2 MHz, V_{IN} = 48 V, and V_{OUT} = 12 V

EPC9105 Bus Converter

EPC9105 Demonstration Board

36 - 60 V_{IN}, 12 V_{OUT}, 350 W, 1.2 MHz





Resonant Converter Summary

- eGaN FETs improve high frequency resonant converter performance
  - Lower output charge
  - Lower gate charge
  - More power delivery per cycle

Summary

- GaN transistors have the potential to replace silicon power MOSFETs in power conversion applications with a low-cost and higher efficiency solution
- eGaN FETs are straightforward to use, but care must be taken due to the higher switching speeds compared with power MOSFETs
- GaN transistors enable exciting new applications such as RF Envelope Tracking